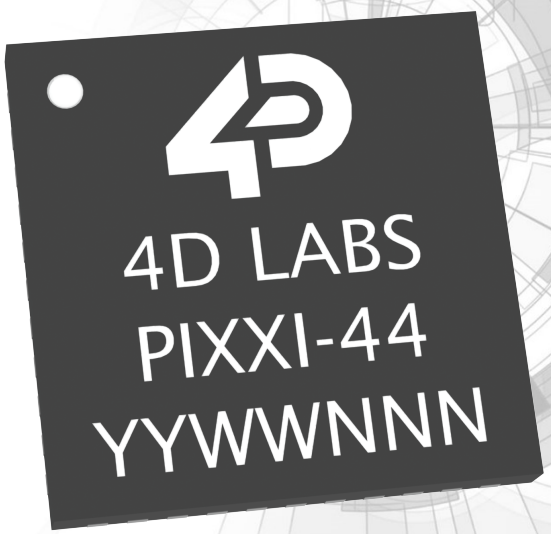
PIXXI-44 Processor

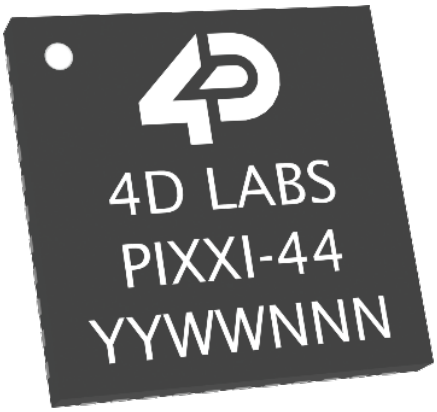


Datasheet

Revision 1.6

Contents

1. Description



The PIXXI-44 processor is a configurable custom graphics controller ideally suited for embedded applications. The chip can be configured to interface with many popular TFT-LCD and OLED displays. Powerful graphics, text, image, animation, hardware peripherals, and countless more features are built right inside the chip. It offers a simple interface to many colour LCD and OLED displays, with or without resistive or capacitive touch panels.

PIXXI-44 has a configurable core layer and hardware layer, which allows it to support LCD modules with various display drivers and touch interfaces. Supported display interfaces include 3-wire and 4-wire serial SPI, MCU 8-bit, and MCU 16-bit display interfaces. On the other hand, supported touch interfaces include 4-wire resistive touch panel interface and capacitive touch panel interface through an I2C touch controller. Configuration of the processor is possible through a powerful, automated software tool that enables the designer to define the core and hardware layers. This design methodology takes away the burden of low-level design, and it offers an enormous advantage in terms of design flexibility, development time, and cost savings.

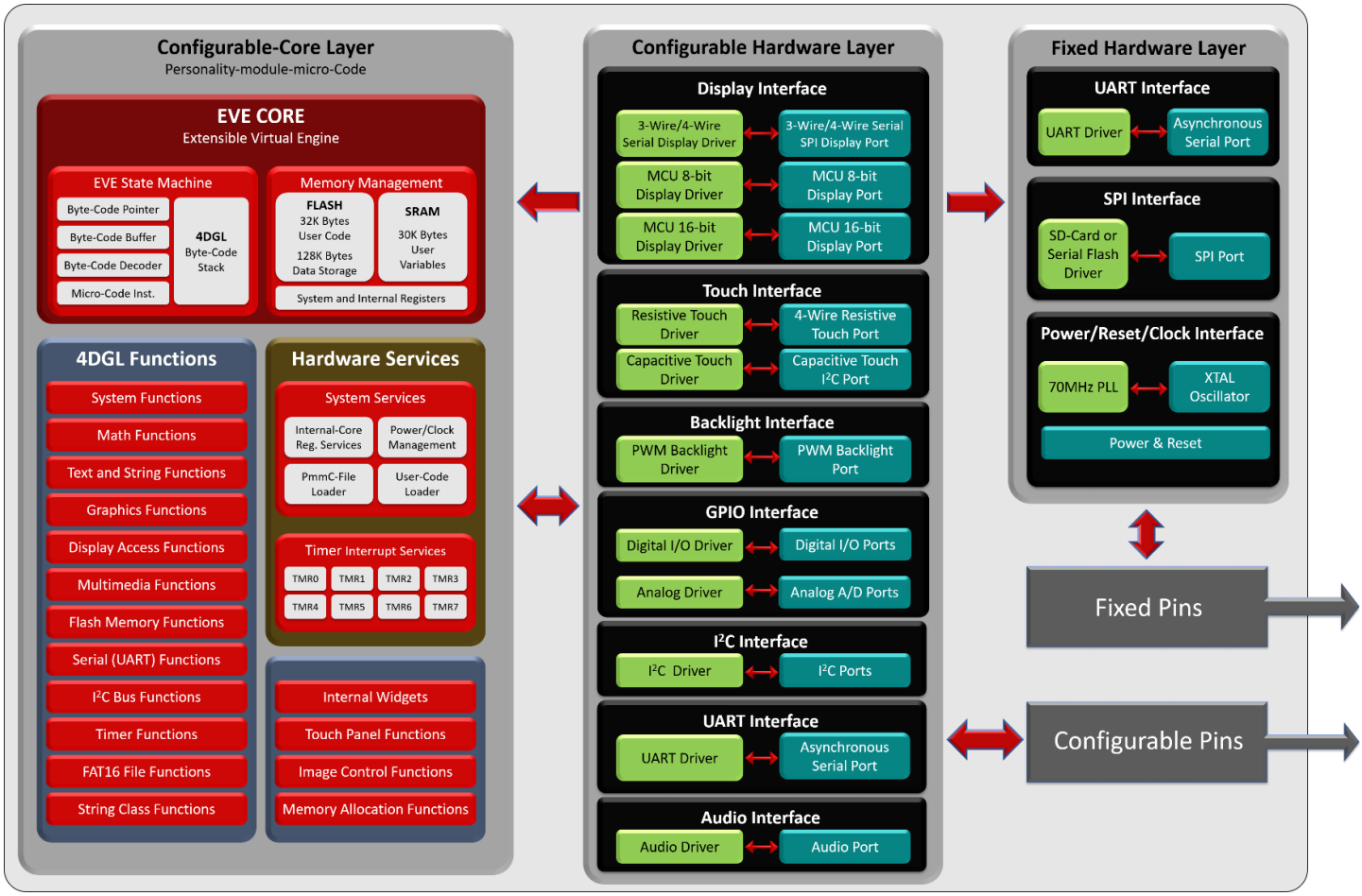
2. Features

- Low-cost TFT-LCD and OLED display graphics user interface solution.
- Ideal as a standalone embedded graphics processor or interface to any low-cost host controller as a graphics co-processor.
- Configurable hardware and core layers which enables support for TFT and OLED with 3-wire and 4-wire serial SPI, MCU 8-bit, and MCU 16-bit interfaces. All data and control signals are provided.
- Configurable hardware and core layers which enables support for 4-Wire Resistive Touch Panel interface and Capacitive Touch Panel interface through an I2C capacitive touch controller.
- Built-in high-performance Processor core (EVE) with an extensive byte-code instruction set optimised for 4DGL, the high level 4D Graphics Language.
- Built-in highly optimised Configurable-Core that takes care of low-level services such as: Display Drivers, Graphics Primitives, Fonts, Multimedia, FAT16 Files, Touch Panel and much more.
- Comprehensive set of built-in graphics and multimedia services that allow users with minimal experience to create high quality graphics applications.
- Display full colour widgets, images, animations, icons and video clips.
- Free comprehensive Software Development Tools (Workshop4) that allows the designer to configure the core and hardware layers. Workshop4 also provides drag and drop widgets for rapid application development.

- Dedicated SPI interface for either SD memory card (SD with up to 2GB or SDHC memory cards starting from 4GB and above) or Serial Flash memory chip (up to 16 MB) for multimedia storage and data logging purposes.
- PWM output pin for backlight LED brightness control.
- 32KB of Flash memory for user application code.
- 30KB of SRAM for user variables.
- 19 General Purpose I/O pins for user interfacing. Depending on the processor mode of configuration, the GPIO pins are variously configurable for alternative functions such as:
    - 4x Analog Input channels
    - 3x I2C ports (master mode, maximum supported speed is fast mode)
    - 1x dedicated and 1x configurable UART ports. Asynchronous hardware serial, with 300 to 2187500 baud. The dedicated UART port is also used for device programming.
- 8 x 16-bit timers with 1 millisecond resolution.
- Audio support (dependent on the processor mode of configuration) for wave files and complex sound generation with a dedicated 16-bit PWM audio output.
- 12MHz oscillator for external crystal with built-in PLL providing 70MHz system clock.
- Single 3.3 Volt Supply (3.0V to 3.6V range).
- -40°C to 85°C extended temperature range.
- Available in a 44-pin QFN 8x8x0.9 mm package.
- RoHS compliant.

3. Block Diagram

The block diagram below is an accurate representation of the chip internals. For a more detailed description on each section please refer to Device Overview section.



Chip Block Diagram

4. Typical Applications

- General purpose low-cost embedded graphics
- Elevator control systems
- Point of sale terminals
- Electronic gauges and metres
- Test and measurement and general-purpose instrumentation
- Industrial control and Robotics
- Automotive system displays
- GPS/Sat-Nav systems
- Medical instruments and applications
- Heart rate and Blood pressure monitors
- Smart Home Automation display panels
- Consumer appliance devices
- Security and Access control panels
- Air conditioner control panels
- Lighting control panels
- Vending machine panels
- Power meter panels
- Gaming equipment
- And much more

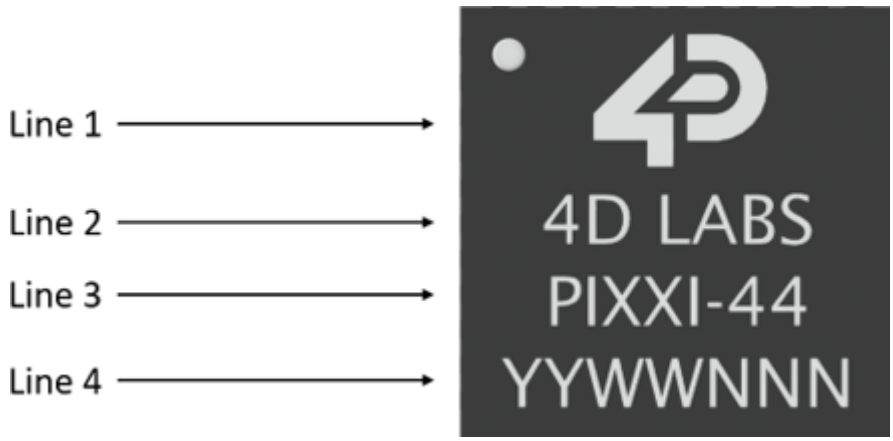
5. Device Information

5.1. Package and Ordering Information

Part Number	Chip Marking	Package Information
4DL-PIXXI-44	PIXXI-44	Package: 44 pin QFN Pin Pitch: 0.65mm Body Size: 8mm x 8mm x 0.9mm

Note

1. Packaging is in reels or cut tapes.
2. Packaging size for reels is 1600 units.



Package Marking

- Line 1: Logo
- Line 2: Company Name
- Line 3: Chip Marking
- Line 4: YY=Year Code, WW=Week Code, NNN=Traceability Code

6. Device Configuration Modes

PIXXI is designed to work with minimal design effort and all of the data and control signals are provided by the chip to interface directly to the display. Simply choose your display, configure PIXXI using the 4D Labs Project editor in Workshop4 IDE according to the desired type of display interface and touch interface, and connect the display to PIXXI on your application board. This offers enormous advantage to the designer in development time, design flexibility, and cost saving and takes away all of the burden of low-level design. For more details pertaining to custom display configuration, please refer to the PIXXI Custom Display Configuration User Manual. The table below shows the different modes by which the PIXXI-44 processor can be configured.

Different Modes of Configuration for PIXXI-44

Mode	Display Interface	Touch Interface Non-Touch	Touch Interface Resistive Touch	Touch Interface Capacitive Touch
Mode-1	3-Wire SPI Display Interface	Mode-1N	Mode-1R	Mode-1C
Mode-2	4-Wire SPI Display Interface	Mode-2N	Mode-2R	Mode-2C
Mode-3	MCU 8-bit Display Interface	Mode-3N	Mode-3R	Mode-3C
Mode-4	MCU 16-bit Display Interface	Mode-4N	Mode-4R	Mode-4C

As can be seen in the table above, there are three different touch interfaces for each configuration/mode of display interface. The following sections discuss these in more detail. The pixel transfer rate for the four different mode is approximately 1.1 million pixels per second.

Note

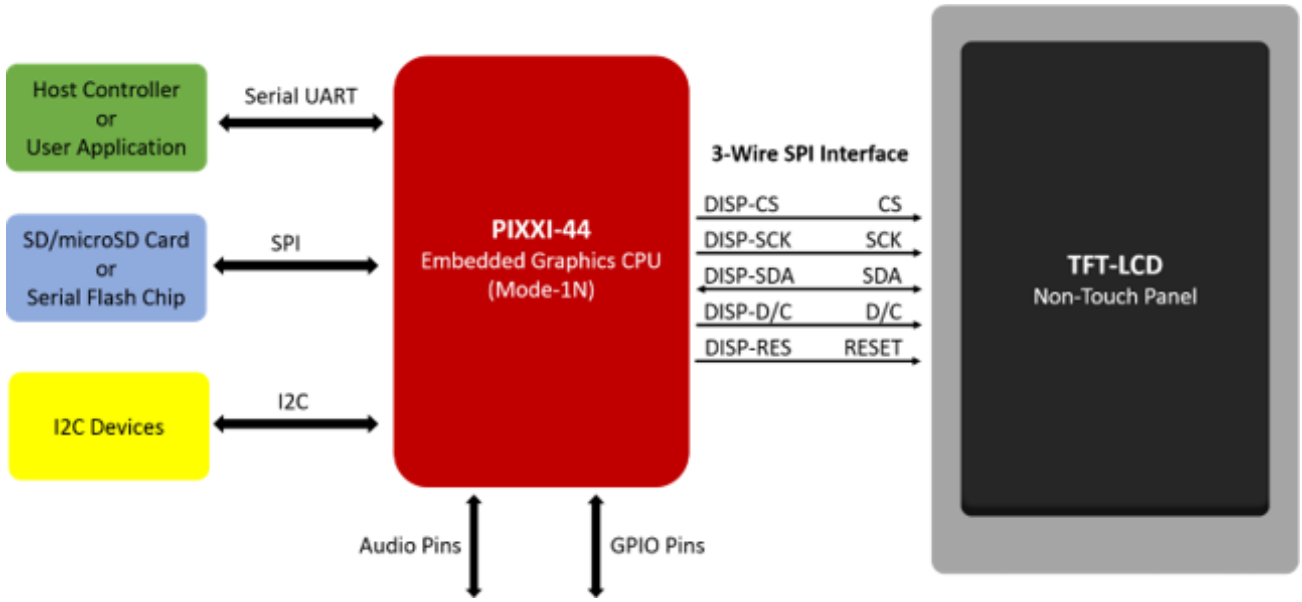
Mode-1 and Mode-3 are currently not implemented with PIXXI-44, but will be available in the future. Mode-2 and Mode-4 are currently the only supported modes.

If your custom application requires one of the currently unavailable modes, please contact our sales team, as it may be possible to be implemented.

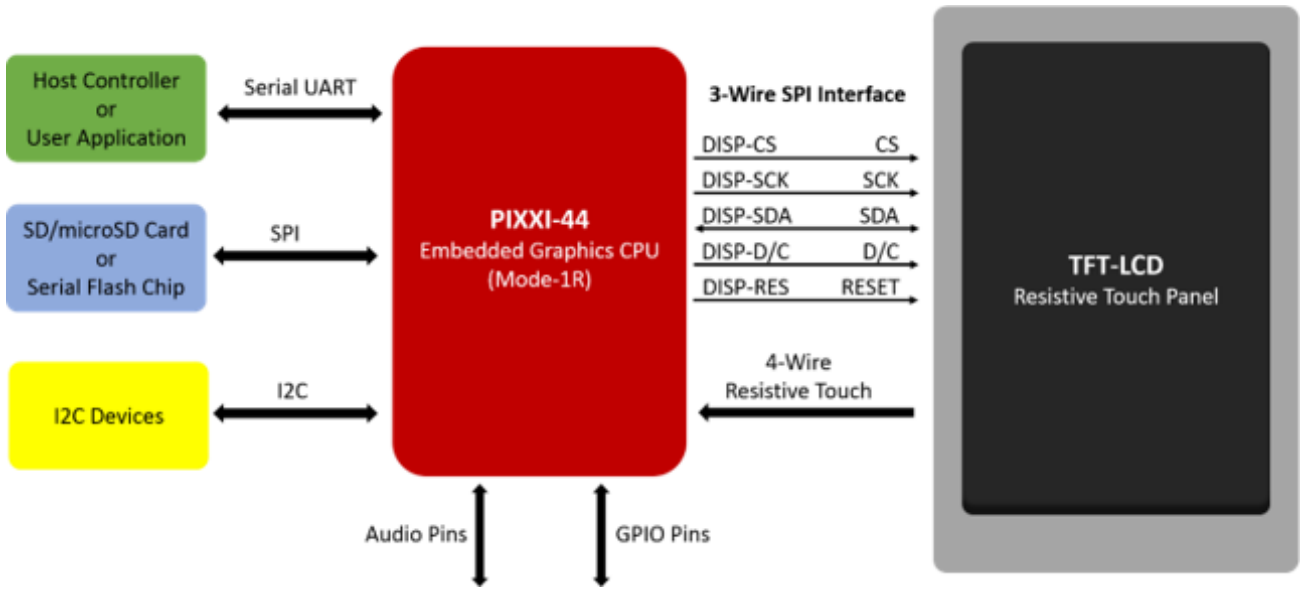
6.1. Mode-1: 3-Wire SPI Display Interface

6.1.1. Block Diagrams

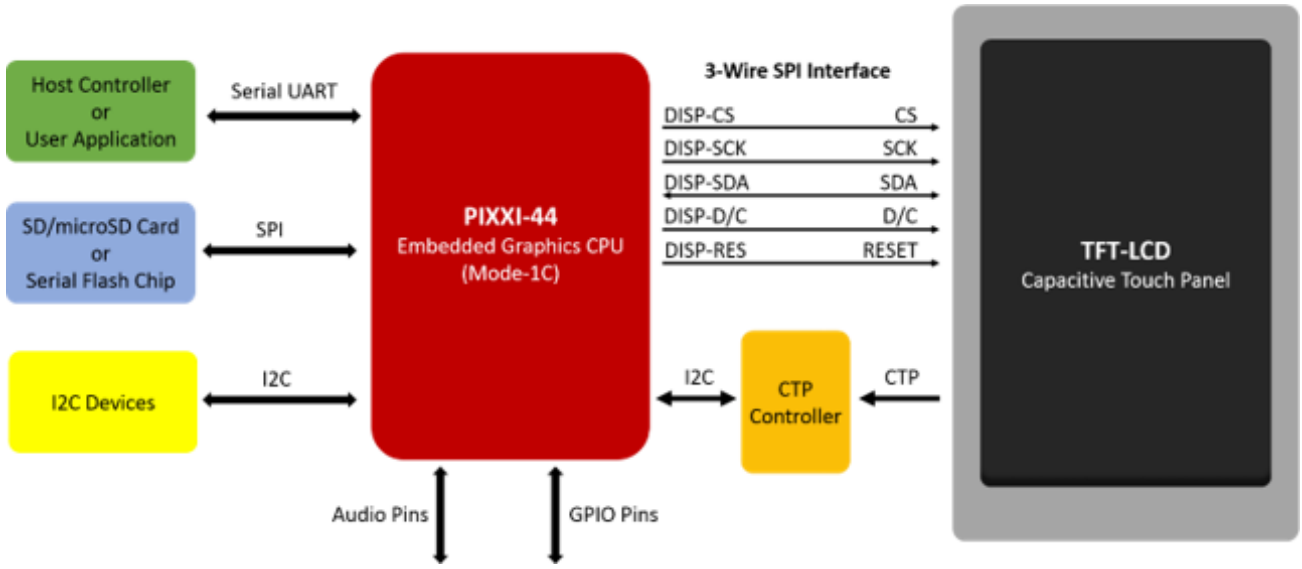
Following block diagrams show the available configurations for different touch panel interfaces under Mode-1.



Block Diagram - Mode-1N: 3-Wire SPI Display Interface, Non-Touch



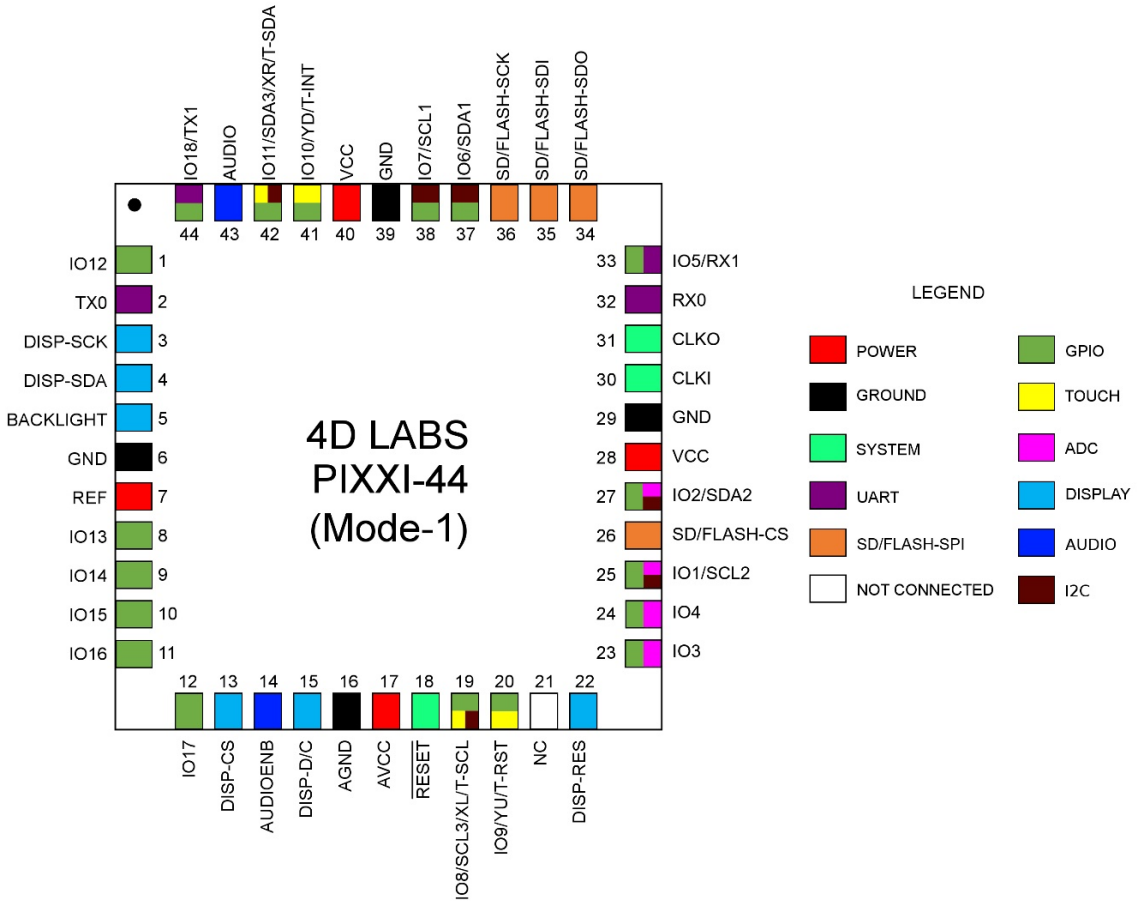
Block Diagram - Mode-1R: 3-Wire SPI Display Interface, Resistive Touch



Block Diagram - Mode-1C: 3-Wire SPI Display Interface, Capacitive Touch

6.1.2. Pin Configuration and Summary

The following diagram and table show the pinout diagram and pin descriptions for Mode-1.



Mode-1 Pinout Diagram

Mode-1 Pinout Description

Pin	Symbol	I/O	Description
1	IO12	I/O	This pin is available as a GPIO pin. This pin outputs 0V or 3.3V levels and is 5.0V tolerant as an input.
2	TX0	O	Dedicated Asynchronous Serial Port Transmit pin, TX0. This pin outputs 3.3V level.
3	DISP-SCK	O	This pin is the DISP-SCK (Display SPI Serial Clock Output signal) pin. Connect this pin to the SPI Serial Clock (SCK) signal of the display. This pin outputs 3.3V level.
4	DISP-SDA	I/O	This pin is the DISP-SDA (Display SPI Serial Data In/Out signal) pin. Connect this pin to the SPI Serial Data In/Out (SDA) signal of the display. This pin outputs 3.3V level and is 5.0V tolerant.
5	BACKLIGHT	O	This pin is the display backlight pin. This pin can output a Pulse Width Modulated (PWM) signal. It can be used with a simple transistor circuit to control backlight LEDs that are in a parallel configuration or it can be used with more complicated DC/DC high voltage circuits for LEDs that have a series configuration. This pin outputs 3.3V. ***High***: Enable DC-DC converter ***Low***: Disable DC-DC converter.
6	GND	P	Device Ground.
7	REF	P	Internal voltage regulator filter capacitor pin. Connect a 4.7uF to 10uF capacitor from this pin to Ground. Position capacitor as close as possible.
8	IO13	I/O	This pin is available as a GPIO pin. This pin outputs 0V or 3.3V levels and is 5.0V tolerant as an input.
9	IO14	I/O	This pin is available as a GPIO pin. This pin outputs 0V or 3.3V levels and is 5.0V tolerant as an input.
10	IO15	I/O	This pin is available as a GPIO pin. This pin outputs 0V or 3.3V levels and is 5.0V tolerant as an input.
11	IO16	I/O	This pin is available as a GPIO pin. This pin outputs 0V or 3.3V levels and is 5.0V tolerant as an input.
12	IO17	I/O	This pin is available as a GPIO pin. This pin outputs 0V or 3.3V levels and is 5.0V tolerant as an input.
13	DISP-CS	O	This pin is the DISP-CS (Display SPI Chip Select signal) pin. Connect this pin to the SPI Chip Select (CS) pin of the display, if needed. This pin outputs 3.3V level.
14	AUDIOENB	O	This pin is Audio Enable pin. Connect this pin to amplifier control. This pin outputs 3.3V level. LOW: Disable external Audio amplifier. HIGH: Enable external Audio amplifier.
15	DISP-D/C	O	This pin is the DISP-D/C (Display Data or Command Select signal) pin. Connect this pin to the Data or Command select (D/C) signal of the display. (3.3V level)
16	AGND	P	Analog Ground.
17	AVCC	P	Analog Positive Supply.
18	RESET	I	Master Reset signal. This pin is 5.0V tolerant. Connect a 4.7K pull-up resistor from this pin to VCC. Active Low.
19	IO8/SCL3/ XL/T-SCL	I/O	**Mode-1N:** This pin is available as a GPIO pin. It can also be configured as an I2C clock output pin, SCL3. This pin outputs 3.3V level and is 3.3V tolerant only. **Mode-1R:** This pin is XL (4-wire resistive touch screen left signal) pin. Connect this pin to XL or X- signal of the touch panel. **Mode-1C:** This pin is T-SCL (I2C Clock Output) pin. Connect this pin to the I2C clock input (SCL) signal of the capacitive touch controller. This pin outputs 3.3V level.

Pin	Symbol	I/O	Description
20	IO9/YU/ T-RST	A/I/O	**Mode-1N:** This pin is available as a GPIO pin. This pin outputs 3.3V level and is 3.3V tolerant only. **Mode-1R:** This pin is YU (4-wire resistive touch screen up signal) pin. Connect this pin to YU or Y+ signal of the touch panel. **Mode-1C:** This pin is T-RST (Touch Reset) pin. Connect this pin to the reset signal of the capacitive touch controller. (3.3V level)
21	NC	I	For 3-wire serial SPI configuration, this pin should be left open.
22	DISP-RES	O	This pin is the DISP-RES (Display RESET signal) pin. Connect this pin to the Reset (RES) signal of the display. This pin outputs 3.3V level.
23	IO3	A/I/O	This pin is available as a General Purpose I/O pin with analog capability. This pin outputs 3.3V level and is 3.3V tolerant only. When used as an analog input, this pin has a range of 0 to 3.3V.
24	IO4/TX1	A/I/O	This pin is available as a General Purpose I/O pin with analog capability. It can also be configured as an asynchronous serial port transmit pin, TX1. This pin outputs 3.3V level and is 3.3V tolerant only. When used as an analog input, this pin has a range of 0 to 3.3V.
25	IO1/SCL2	A/I/O	This pin is available as a General Purpose I/O pin with analog capability. It can also be configured as an I2C clock output pin, SCL2. This pin outputs 3.3V level and is 3.3V tolerant only. When used as an analog input, this pin has a range of 0 to 3.3V.
26	SD/ FLASH-CS	O	SD/FLASH SPI Serial Chip Select. SD memory card or serial flash memory chip use only. Connect this pin to the SPI Chip Select (CS) signal of the memory device. This pin outputs 3.3V level.
27	IO2/SDA2	A/I/O	This pin is available as a General Purpose I/O pin with analog capability. It can also be configured as an I2C Data In/Out pin, SDA2. This pin outputs 3.3V level and is 3.3V tolerant only. When used as an analog input, this pin has a range of 0 to 3.3V.
28	VCC	P	Device Positive Supply.
29	GND	P	Device Ground.
30	CLKI	I	Device Clock input 1 of a 12MHz crystal.
31	CLKO	O	Device Clock input 2 of a 12MHz crystal.
32	RX0	I	Dedicated Asynchronous Serial Port Receive pin, RX0. This pin is 5.0V tolerant.
33	IO5/RX1	I/O	This pin is available as a General Purpose I/O pin. It can also be configured as an asynchronous serial port receive pin, RX1. This pin outputs 3.3V level and is 5.0V tolerant.
34	SD/ FLASH-SDO	O	SD/FLASH SPI Serial Data Output. SD memory card or serial flash memory chip use only. Connect this pin to the SPI Serial Data In (SDI) signal of the memory device. This pin outputs 3.3V level.
35	SD/ FLASH-SDI	I	SD/FLASH SPI Serial Data Input. SD memory card or serial flash memory chip use only. Connect this pin to the SPI Serial Data Out (SDO) signal of the memory device. This pin is 3.3V tolerant.
36	SD/ FLASH-SCK	O	SD/FLASH SPI Serial Clock output. SD memory card or serial flash memory chip use only. Connect this pin to the SPI Serial Clock (SCK) signal of the memory device. This pin outputs 3.3V level.
37	IO6/SDA1	I/O	This pin is available as a General Purpose I/O pin. It can also be configured as an I2C Data In/Out pin, SDA1. This pin outputs 3.3V level and is 3.3V tolerant.
38	IO7/SCL1	I/O	This pin is available as a General Purpose I/O pin. It can also be configured as an I2C clock output pin, SCL1. This pin outputs 3.3V level and is 3.3V tolerant.
39	GND	P	Device Ground.

Pin	Symbol	I/O	Description
40	VCC	P	Device Positive Supply.
41	IO10/YD/ T-INT	I/O	**Mode-1N:** This pin is available as a GPIO pin. This pin outputs 0V or 3.3V levels and is 5.0V tolerant as an input. **Mode-1R:** This pin is YD (4-wire resistive touch screen bottom signal) pin. Connect this pin to YD or Y- signal of the touch panel. **Mode-1C:** This pin is T-INT (touch interrupt signal) pin. Connect this pin to the interrupt signal pin of the capacitive touch controller. This pin is 5.0V tolerant.
42	IO11/SDA3/ XR/T-SDA	A/I/O	**Mode-1N:** This pin is available as a GPIO pin. It can also be configured as an I2C Data In/Out pin, SDA3. This pin outputs 3.3V level and is 5.0V tolerant. **Mode-1R:** This pin is XR (4-wire resistive touch screen right signal) pin. Connect this pin to XR or X+ signal of the touch panel. **Mode-1C:** This pin is T-SDA (I2C Data In/Out) pin. Connect this pin to the I2C data in/ out signal (SDA) of the capacitive touch controller. This pin outputs 3.3V level and is 5.0V tolerant.
43	AUDIO	O	This pin is the Pulse Width Modulated (PWM) Audio output pin. Connect this pin to a 2-stage low pass filter then into an audio amplifier.
44	IO18	I/O	This pin is available as a GPIO pin. This pin outputs 3.3V level and is 3.3V tolerant only.

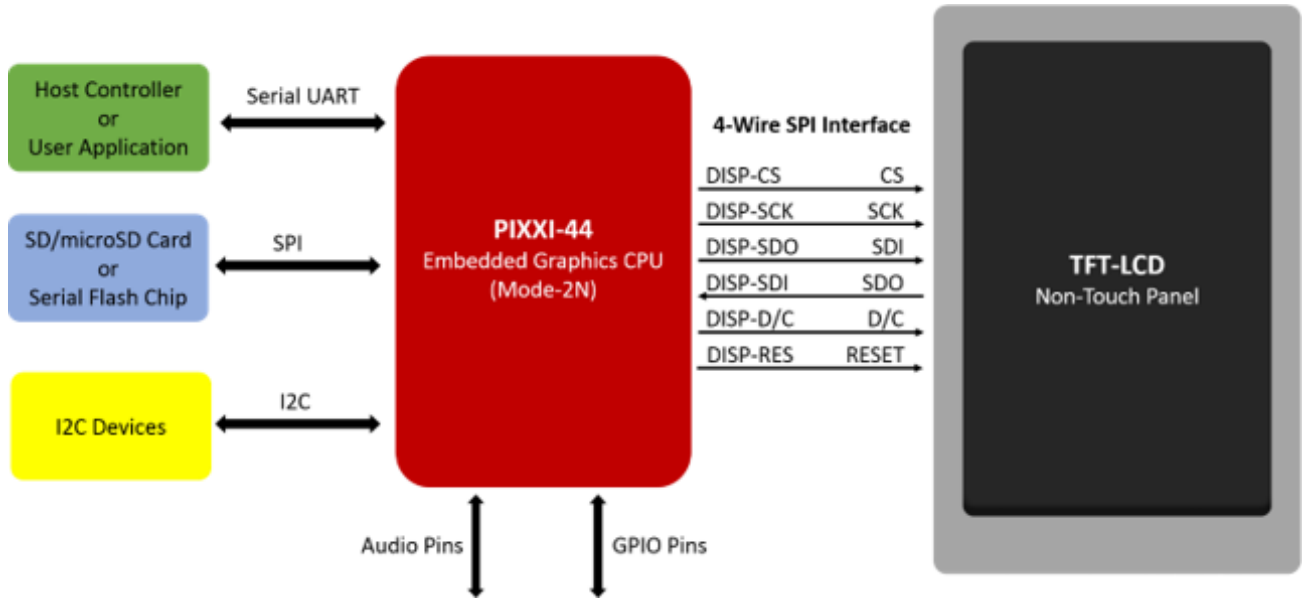
Note

I = Input, **O** = Output, **P** = Power, **A** = Analogue

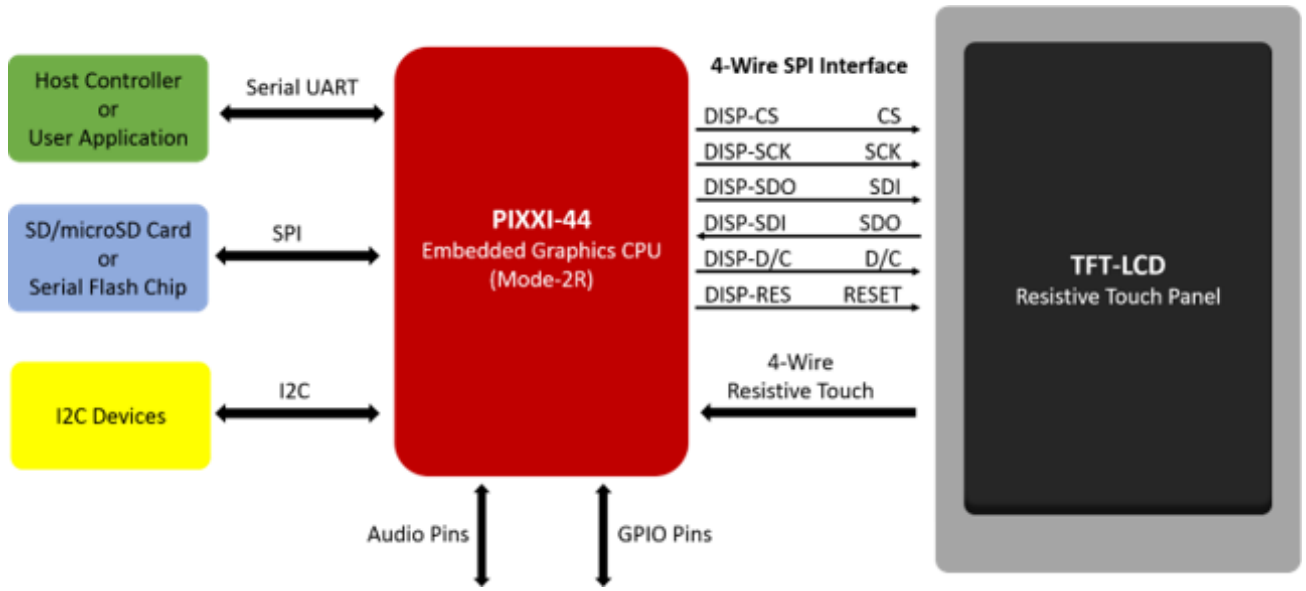
6.2. Mode-2: 4-Wire SPI Display Interface

6.2.1. Block Diagrams

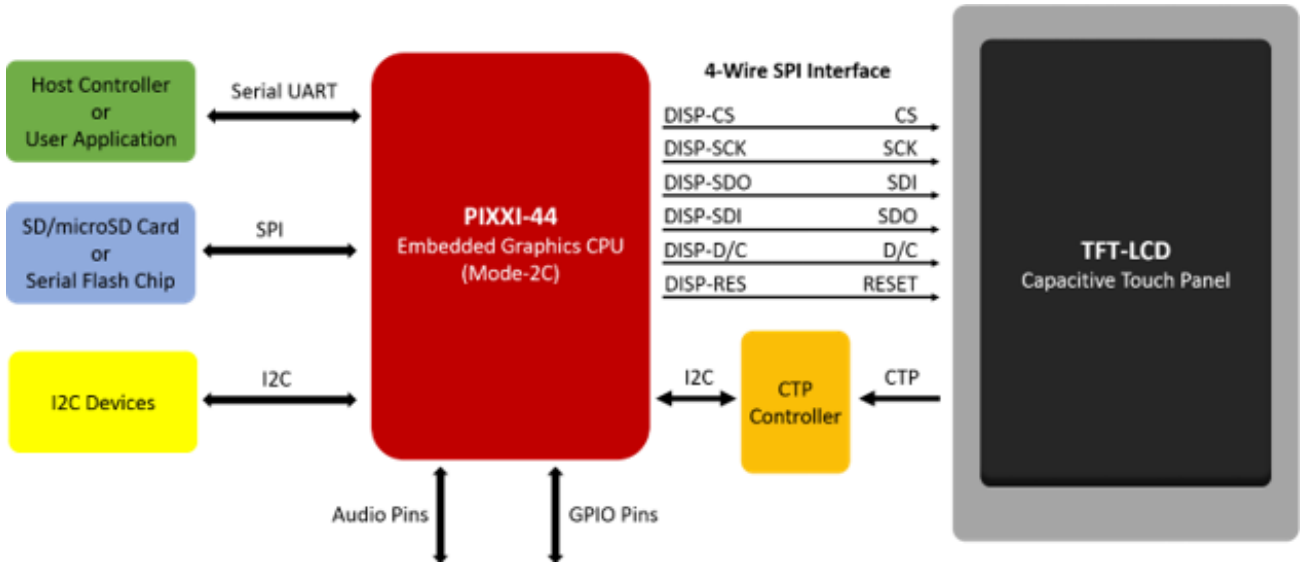
Following block diagrams show the available configurations for different touch panel interfaces under Mode-2.



Block Diagram - Mode-2N: 4-Wire SPI Display Interface, Non-Touch



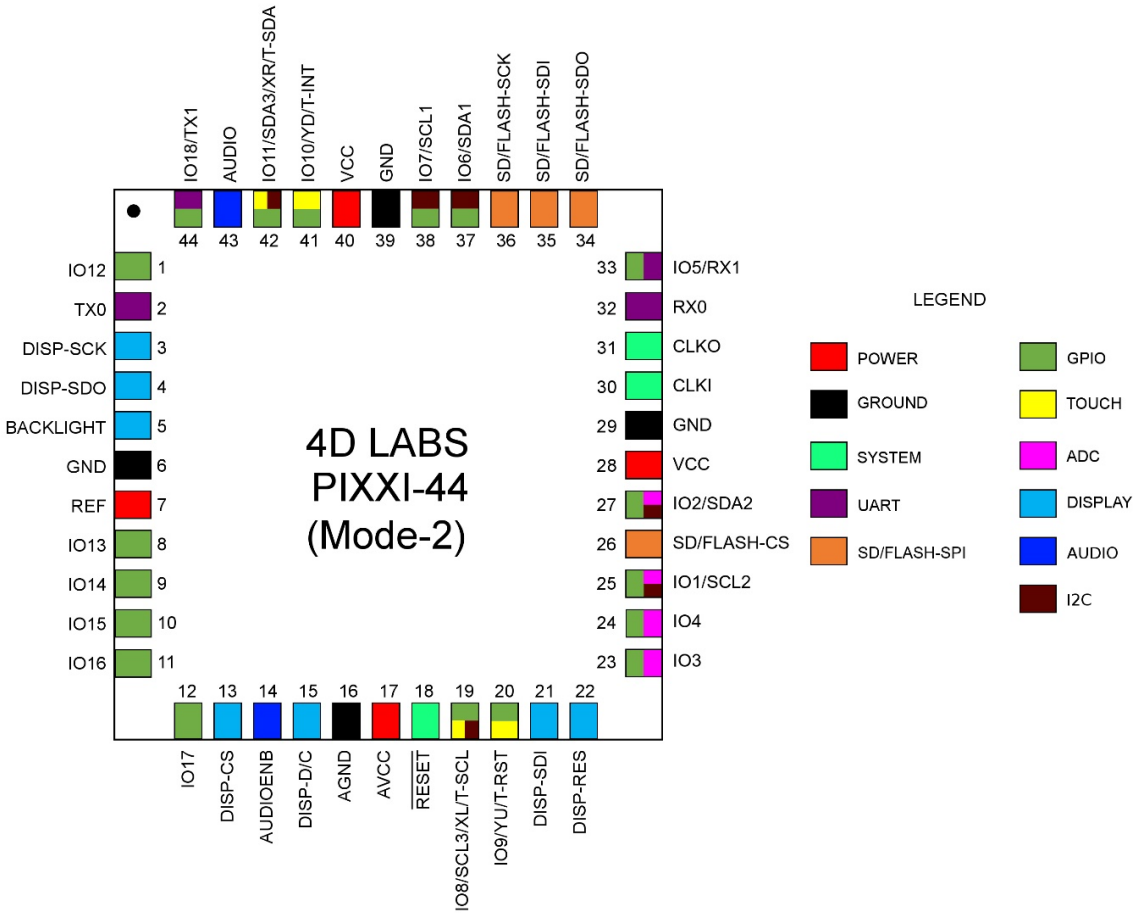
Block Diagram - Mode-2R: 4-Wire SPI Display Interface, Resistive Touch



Block Diagram - Mode-2C: 4-Wire SPI Display Interface, Capacitive Touch

6.2.2. Pin Configuration and Summary

The following diagram and table show the pinout diagram and pin descriptions for Mode-2.



Mode-2 Pinout Diagram

Mode-2 Pinout Description

Pin	Symbol	I/O	Description
1	IO12	I/O	This pin is available as a GPIO pin. This pin outputs 0V or 3.3V levels and is 5.0V tolerant as an input.
2	TX0	O	Dedicated Asynchronous Serial Port Transmit pin, TX0. This pin outputs 3.3V level.
3	DISP-SCK	O	This pin is the DISP-SCK (Display SPI Serial Clock Output signal) pin. Connect this pin to the SPI Serial Clock (SCK) signal of the display. This pin outputs 3.3V level.
4	DISP-SDO	O	This pin is the DISP-SDO (Display SPI Serial Data Out signal) pin. Connect this pin to the SPI Serial Data In (SDI) signal of the display. This pin outputs 3.3V level and is 5.0V tolerant.
5	BACKLIGHT	O	This pin is the display backlight pin. This pin can output a Pulse Width Modulated (PWM) signal. It can be used with a simple transistor circuit to control backlight LEDs that are in a parallel configuration or it can be used with more complicated DC/DC high voltage circuits for LEDs that have a series configuration. This pin outputs 3.3V level. High: Enable DC-DC converter. Low: Disable DC-DC converter.
6	GND	P	Device Ground.
7	REF	P	Internal voltage regulator filter capacitor pin. Connect a 4.7uF to 10uF capacitor from this pin to Ground. Position capacitor as close as possible.
8	IO13	I/O	This pin is available as a GPIO pin. This pin outputs 0V or 3.3V levels and is 5.0V tolerant as an input.
9	IO14	I/O	This pin is available as a GPIO pin. This pin outputs 0V or 3.3V levels and is 5.0V tolerant as an input.
10	IO15	I/O	This pin is available as a GPIO pin. This pin outputs 0V or 3.3V levels and is 5.0V tolerant as an input.
11	IO16	I/O	This pin is available as a GPIO pin. This pin outputs 0V or 3.3V levels and is 5.0V tolerant as an input.
12	IO17	I/O	This pin is available as a GPIO pin. This pin outputs 0V or 3.3V levels and is 5.0V tolerant as an input.
13	DISP-CS	O	This pin is the DISP-CS (Display SPI Chip Select signal) pin. Connect this pin to the SPI Chip Select (CS) pin of the display, if needed. This pin outputs 3.3V level.
14	AUDIOENB	O	This pin is Audio Enable pin. Connect this pin to amplifier control. (3.3V level) LOW: Disable external Audio amplifier. HIGH: Enable external Audio amplifier.
15	DISP-D/C	O	This pin is the DISP-D/C (Display Data or Command Select signal) pin. Connect this pin to the Data or Command select (D/C) signal of the display. This pin outputs 3.3V.
16	AGND	P	Analog Ground.
17	AVCC	P	Analog Positive Supply.
18	RESET	I	Master Reset signal. This pin is 5.0V tolerant. Connect a 4.7K pull-up resistor from this pin to VCC. Active Low.
19	IO8/SCL3/ XL/T-SCL	I/O	**Mode-2N:** This pin is available as a GPIO pin. It can also be configured as an I2C clock output pin, SCL3. This pin outputs 3.3V level and is 3.3V tolerant only. **Mode-2R:** This pin is XL (4-wire resistive touch screen left signal) pin. Connect this pin to XL or X- signal of the touch panel. **Mode-2C:** This pin is T-SCL (I2C Clock Output) pin. Connect this pin to the I2C clock input (SCL) signal of the capacitive touch controller. This pin outputs 3.3V level.

Pin	Symbol	I/O	Description
20	IO9/YU/ T-RST	A/I/O	**Mode-2N:** This pin is available as a GPIO pin. This pin outputs 3.3V level and is 3.3V tolerant only. **Mode-2R:** This pin is YU (4-wire resistive touch screen up signal) pin. Connect this pin to YU or Y+ signal of the touch panel. **Mode-2C:** This pin is T-RST (Touch Reset) pin. Connect this pin to the reset signal of the capacitive touch controller. (3.3V level)
21	DISP-SDI	I	For 4-wire serial SPI configuration, this pin is the DISP-SDI (Display SPI Serial Data In signal) pin. Connect this pin to the SPI Serial Data Out (SDO) signal of the display. This pin is 3.3V tolerant only.
22	DISP-RES	O	This pin is the DISP-RES (Display RESET signal) pin. Connect this pin to the Reset (RES) signal of the display. This pin outputs 3.3V level.
23	IO3	A/I/O	This pin is available as a General Purpose I/O pin with analog capability. This pin outputs 3.3V level and is 3.3V tolerant only. When used as an analog input, this pin has a range of 0 to 3.3V.
24	IO4	A/I/O	This pin is available as a General Purpose I/O pin with analog capability. This pin outputs 3.3V level and is 3.3V tolerant only. When used as an analog input, this pin has a range of 0 to 3.3V.
25	IO1/SCL2	A/I/O	This pin is available as a General Purpose I/O pin with analog capability. It can also be configured as an I2C clock output pin, SCL2. This pin outputs 3.3V level and is 3.3V tolerant only. When used as an analog input, this pin has a range of 0 to 3.3V.
26	SD/ FLASH-CS	O	SD/FLASH SPI Serial Chip Select. SD memory card or serial flash memory chip use only. Connect this pin to the SPI Chip Select (CS) signal of the memory device. This pin outputs 3.3V level.
27	IO2/SDA2	A/I/O	This pin is available as a General Purpose I/O pin with analog capability. It can also be configured as an I2C Data In/Out pin, SDA2. This pin outputs 3.3V level and is 3.3V tolerant only. When used as an analog input, this pin has a range of 0 to 3.3V.
28	VCC	P	Device Positive Supply.
29	GND	P	Device Ground.
30	CLKI	I	Device Clock input 1 of a 12MHz crystal.
31	CLKO	O	Device Clock input 2 of a 12MHz crystal.
32	RX0	I	Dedicated Asynchronous Serial Port Receive pin, RX0. This pin is 5.0V tolerant.
33	IO5/RX1	I/O	This pin is available as a General Purpose I/O pin. It can also be configured as an asynchronous serial port receive pin, RX1. This pin outputs 3.3V level and is 5.0V tolerant.
34	SD/ FLASH-SDO	O	SD/FLASH SPI Serial Data Output. SD memory card or serial flash memory chip use only. Connect this pin to the SPI Serial Data In (SDI) signal of the memory device. This pin outputs 3.3V level.
35	SD/ FLASH-SDI	I	SD/FLASH SPI Serial Data Input. SD memory card or serial flash memory chip use only. Connect this pin to the SPI Serial Data Out (SDO) signal of the memory device. This pin is 3.3V tolerant.
36	SD/ FLASH-SCK	O	SD/FLASH SPI Serial Clock output. SD memory card or serial flash memory chip use only. Connect this pin to the SPI Serial Clock (SCK) signal of the memory device. This pin outputs 3.3V level.
37	IO6/SDA1	I/O	This pin is available as a General Purpose I/O pin. It can also be configured as an I2C Data In/Out pin, SDA1. This pin outputs 3.3V level and is 3.3V tolerant.
38	IO7/SCL1	I/O	This pin is available as a General Purpose I/O pin. It can also be configured as an I2C clock output pin, SCL1. This pin outputs 3.3V level and is 3.3V tolerant.

Pin	Symbol	I/O	Description
39	GND	P	Device Ground.
40	VCC	P	Device Positive Supply.
41	IO10/YD/ T-INT	I/O	**Mode-2N:** This pin is available as a GPIO pin. This pin outputs 0V or 3.3V levels and is 5.0V tolerant as an input. **Mode-2R:** This pin is YD (4-wire resistive touch screen bottom signal) pin. Connect this pin to YD or Y- signal of the touch panel. **Mode-2C:** This pin is T-INT (touch interrupt signal) pin. Connect this pin to the interrupt signal pin of the capacitive touch controller. This pin is 5.0V tolerant.
42	IO11/SDA3/ XR/T-SDA	A/I/O	**Mode-2N:** This pin is available as a GPIO pin. It can also be configured as an I2C Data In/Out pin, SDA3. This pin outputs 3.3V level and is 5.0V tolerant. **Mode-2R:** This pin is XR (4-wire resistive touch screen right signal) pin. Connect this pin to XR or X+ signal of the touch panel. **Mode-2C:** This pin is T-SDA (I2C Data In/Out) pin. Connect this pin to the I2C data in/ out signal (SDA) of the capacitive touch controller. This pin outputs 3.3V level and is 5.0V tolerant.
43	AUDIO	O	This pin is the Pulse Width Modulated (PWM) Audio output pin. Connect this pin to a 2-stage low pass filter then into an audio amplifier.
44	IO18/TX1	I/O	This pin is available as a GPIO pin. It can also be configured as an asynchronous serial port transmit pin, TX1. This pin outputs 3.3V level and is 3.3V tolerant only.

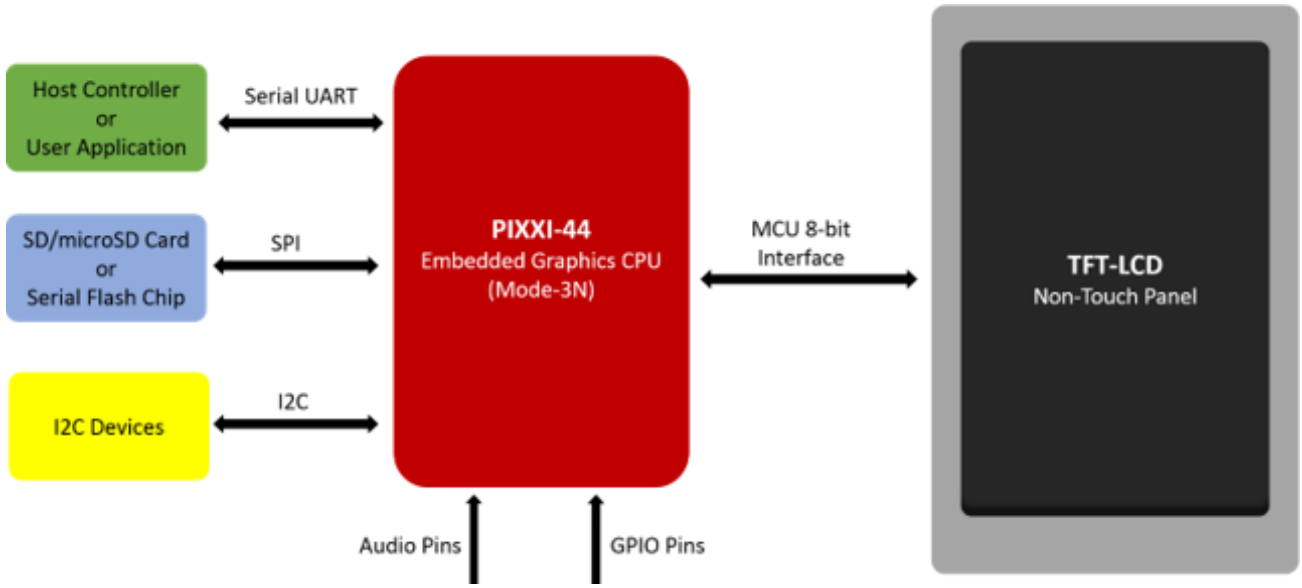
Note

I = Input, **O** = Output, **P** = Power, **A** = Analogue

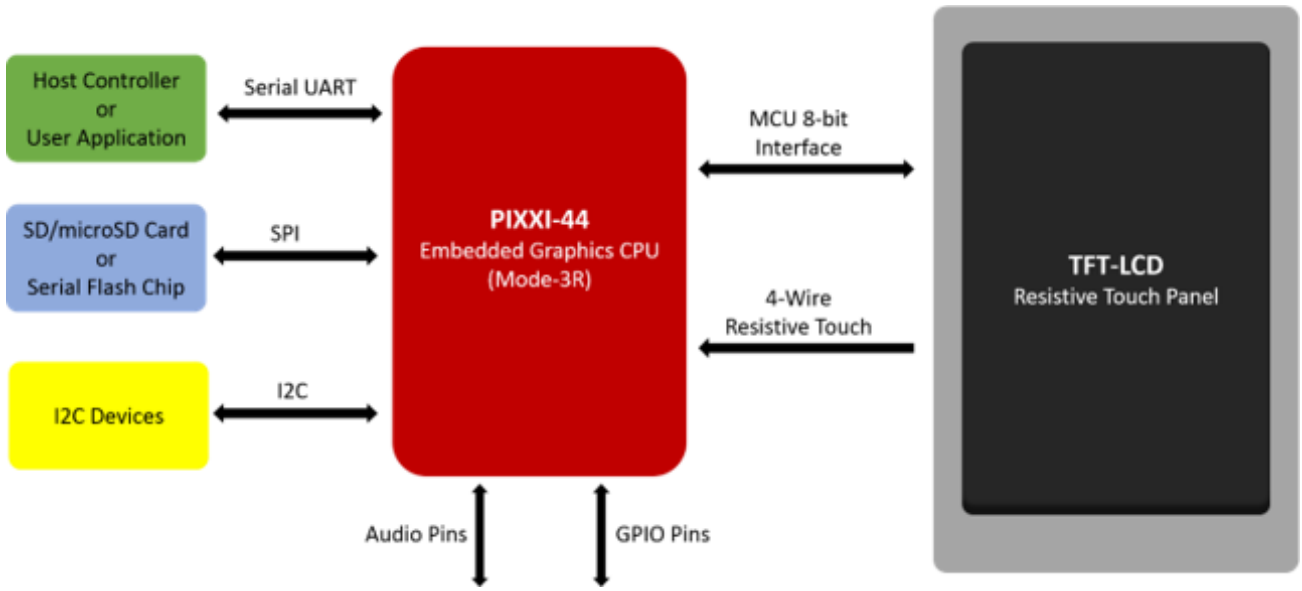
6.3. Mode-3: MCU 8-bit Display Interface

6.3.1. Block Diagrams

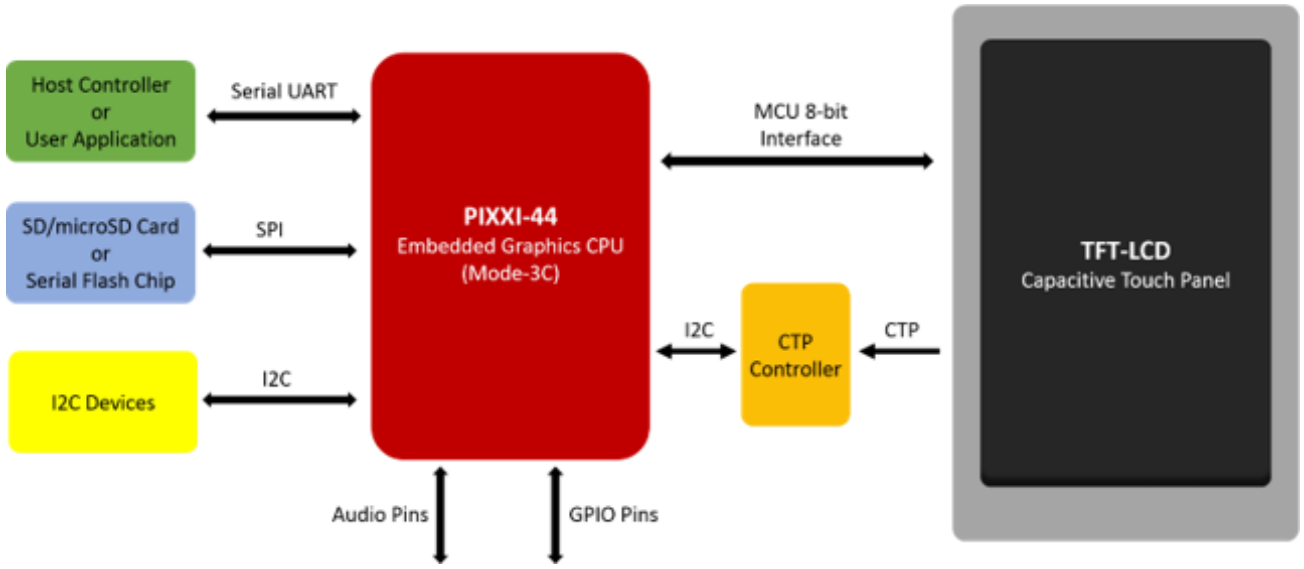
Following block diagrams show the available configurations for different touch panel interfaces under Mode-3.



Block Diagram - Mode-3N: MCU 8-bit Display Interface, Non-Touch



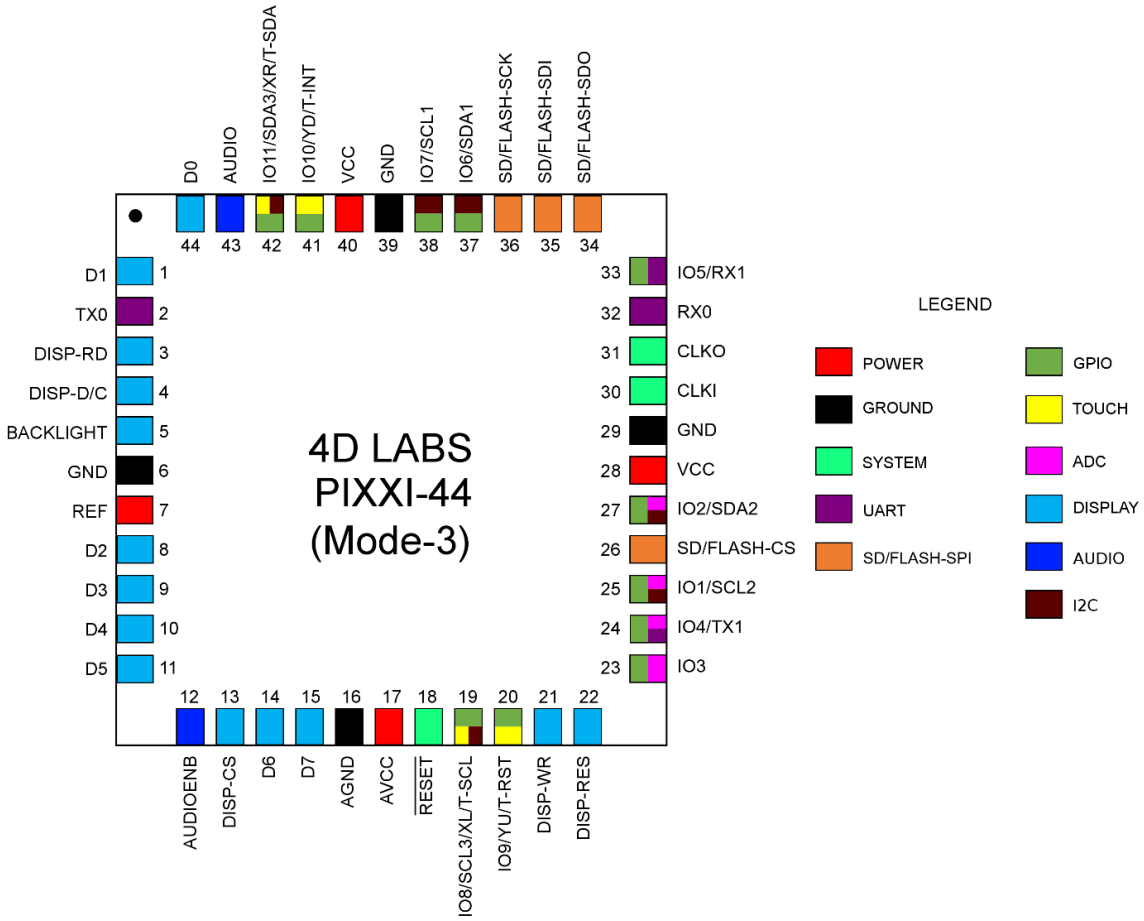
Block Diagram - Mode-3R: MCU 8-bit Display Interface, Resistive Touch



Block Diagram - Mode-3C: MCU 8-bit Display Interface, Capacitive Touch

6.3.2. Pin Configuration and Summary

The following diagram and table show the pinout diagram and pin descriptions for Mode-3.



Mode-3 Pinout Diagram

Mode-3 Pinout Description

Pin	Symbol	I/O	Description
1	D1	I/O	This pin is Display Data Bus bit 1. This pin outputs 3.3V level and is 5.0V tolerant.
2	TX0	O	Dedicated Asynchronous Serial Port Transmit pin, TX0. This pin outputs 3.3V level.
3	DISP-RD	O	This pin is the Display Read strobe signal. PIXXI-44 asserts this signal low when reading data from the display. Connect this pin to the Read (RD) signal of the display. This pin outputs 3.3V level.
4	DISP-D/C	O	This pin is the Display Register Select signal. Connect this pin to the Register Select (RS or A0 or C/D or similar naming convention) signal of the display. (3.3V level) LOW: Display index or status register is selected. HIGH: Display GRAM or register data is selected.
5	BACKLIGHT	O	This pin is the display backlight pin. This pin can output a Pulse Width Modulated (PWM) signal. It can be used with a simple transistor circuit to control backlight LEDs that are in a parallel configuration or it can be used with more complicated DC/DC high voltage circuits for LEDs that have a series configuration. (3.3V level) High: Enable DC-DC converter. Low: Disable DC-DC converter.
6	GND	P	Device Ground.
7	REF	P	Internal voltage regulator filter capacitor pin. Connect a 4.7uF to 10uF capacitor from this pin to Ground. Position capacitor as close as possible.
8	D2	I/O	This pin is Display Data Bus bit 2. This pin outputs 3.3V level and is 5.0V tolerant.
9	D3	I/O	This pin is Display Data Bus bit 3. This pin outputs 3.3V level and is 5.0V tolerant.
10	D4	I/O	This pin is Display Data Bus bit 4. This pin outputs 3.3V level and is 5.0V tolerant.
11	D5	I/O	This pin is Display Data Bus bit 5. This pin outputs 3.3V level and is 5.0V tolerant.
12	AUDIOENB	O	This pin is Audio Enable pin. Connect this pin to amplifier control. (3.3V level) LOW: Disable external Audio amplifier. HIGH: Enable external Audio amplifier.
13	DISP-CS	O	This pin is the DISP-CS (Display Chip Select) signal. Connect this pin to the Chip Select (CS) pin of the display, if needed. This pin outputs 3.3V level.
14	D6	I/O	This pin is Display Data Bus bit 6. This pin outputs 3.3V level and is 5.0V tolerant.
15	D7	I/O	This pin is Display Data Bus bit 7. This pin outputs 3.3V level and is 5.0V tolerant.
16	AGND	P	Analog Ground.
17	AVCC	P	Analog Positive Supply.
18	RESET	I	Master Reset signal. This pin is 5.0V tolerant. Connect a 4.7K pull-up resistor from this pin to VCC. Active Low.
19	IO8/SCL3/ XL/T-SCL	I/O	**Mode-3N:** This pin is available as a GPIO pin. It can also be configured as an I2C clock output pin, SCL3. This pin outputs 3.3V level and is 3.3V tolerant only. **Mode-3R:** This pin is XL (4-wire resistive touch screen left signal) pin. Connect this pin to XL or X- signal of the touch panel. **Mode-3C:** This pin is T-SCL (I2C Clock Output) pin. Connect this pin to the I2C clock input (SCL) signal of the capacitive touch controller. This pin outputs 3.3V level.
20	IO9/YU/ T-RST	A/I/O	**Mode-3N:** This pin is available as a GPIO pin. This pin outputs 3.3V level and is 3.3V tolerant only. **Mode-3R:** This pin is YU (4-wire resistive touch screen up signal) pin. Connect this pin to YU or Y+ signal of the touch panel. **Mode-3C:** This pin is T-RST (Touch Reset) pin. Connect this pin to the reset signal of the capacitive touch controller. This pin outputs 3.3V level.

Pin	Symbol	I/O	Description
21	DISP-WR	O	This pin is the Display Write strobe signal. PIXXI-44 asserts this signal low when writing data to the display. Connect this pin to the Write (WR) signal of the display. This pin outputs 3.3V level
22	DISP-RES	O	This pin is the Display Reset signal. PIXXI-44 initialises the display by strobing this pin low. Connect this pin to the Reset (RES) signal of the display. This pin outputs 3.3V level.
23	IO3	A/I/O	This pin is available as a General Purpose I/O pin with analog capability. This pin outputs 3.3V level and is 3.3V tolerant only. When used as an analog input, this pin has a range of 0 to 3.3V.
24	IO4/TX1	A/I/O	This pin is available as a General Purpose I/O pin with analog capability. It can also be configured as an asynchronous serial port transmit pin, TX1. This pin outputs 3.3V level and is 3.3V tolerant only. When used as an analog input, this pin has a range of 0 to 3.3V.
25	IO1/SCL2	A/I/O	This pin is available as a General Purpose I/O pin with analog capability. It can also be configured as an I2C clock output pin, SCL2. This pin outputs 3.3V level and is 3.3V tolerant only. When used as an analog input, this pin has a range of 0 to 3.3V.
26	SD/ FLASH-CS	O	SD/FLASH SPI Serial Chip Select. SD memory card or serial flash memory chip use only. Connect this pin to the SPI Chip Select (CS) signal of the memory device. This pin outputs 3.3V level.
27	IO2/SDA2	A/I/O	This pin is available as a General Purpose I/O pin with analog capability. It can also be configured as an I2C Data In/Out pin, SDA2. This pin outputs 3.3V level and is 3.3V tolerant only. When used as an analog input, this pin has a range of 0 to 3.3V.
28	VCC	P	Device Positive Supply.
29	GND	P	Device Ground.
30	CLKI	I	Device Clock input 1 of a 12MHz crystal.
31	CLKO	O	Device Clock input 2 of a 12MHz crystal.
32	RX0	I	Dedicated Asynchronous Serial Port Receive pin, RX0. This pin is 5.0V tolerant.
33	IO5/RX1	I/O	This pin is available as a General Purpose I/O pin. It can also be configured as an asynchronous serial port receive pin, RX1. This pin outputs 3.3V level and is 5.0V tolerant.
34	SD/ FLASH-SDO	O	SD/FLASH SPI Serial Data Output. SD memory card or serial flash memory chip use only. Connect this pin to the SPI Serial Data In (SDI) signal of the memory device. This pin outputs 3.3V level.
35	SD/ FLASH-SDI	I	SD/FLASH SPI Serial Data Input. SD memory card or serial flash memory chip use only. Connect this pin to the SPI Serial Data Out (SDO) signal of the memory device. This pin is 3.3V tolerant.
36	SD/ FLASH-SCK	O	SD/FLASH SPI Serial Clock output. SD memory card or serial flash memory chip use only. Connect this pin to the SPI Serial Clock (SCK) signal of the memory device. This pin outputs 3.3V level.
37	IO6/SDA1	I/O	This pin is available as a General Purpose I/O pin. It can also be configured as an I2C Data In/Out pin, SDA1. This pin outputs 3.3V level and is 3.3V tolerant.
38	IO7/SCL1	I/O	This pin is available as a General Purpose I/O pin. It can also be configured as an I2C clock output pin, SCL1. This pin outputs 3.3V level and is 3.3V tolerant.
39	GND	P	Device Ground.
40	VCC	P	Device Positive Supply.
41	IO10/YD/ T-INT	I/O	**Mode-3N:** This pin is available as a GPIO pin. This pin outputs 0V or 3.3V levels and is 5.0V tolerant as an input.

Pin	Symbol	I/O	Description
			Mode-3R: This pin is YD (4-wire resistive touch screen bottom signal) pin. Connect this pin to YD or Y- signal of the touch panel. **Mode-3C:** This pin is T-INT (touch interrupt signal) pin. Connect this pin to the interrupt signal pin of the capacitive touch controller. This pin is 5.0V tolerant.
42	IO11/SDA3/ XR/T-SDA	A/I/O	**Mode-3N:** This pin is available as a GPIO pin. It can also be configured as an I2C Data In/Out pin, SDA3. This pin outputs 3.3V level and is 5.0V tolerant. **Mode-3R:** This pin is XR (4-wire resistive touch screen right signal) pin. Connect this pin to XR or X+ signal of the touch panel. **Mode-3C:** This pin is T-SDA (I2C Data In/Out) pin. Connect this pin to the I2C data in/ out signal (SDA) of the capacitive touch controller. This pin outputs 3.3V level and is 5.0V tolerant.
43	AUDIO	O	This pin is the Pulse Width Modulated (PWM) Audio output pin. Connect this pin to a 2-stage low pass filter then into an audio amplifier.
44	D0	I/O	This pin is Display Data Bus bit 0. This pin outputs 3.3V level and is 3.3V tolerant only.

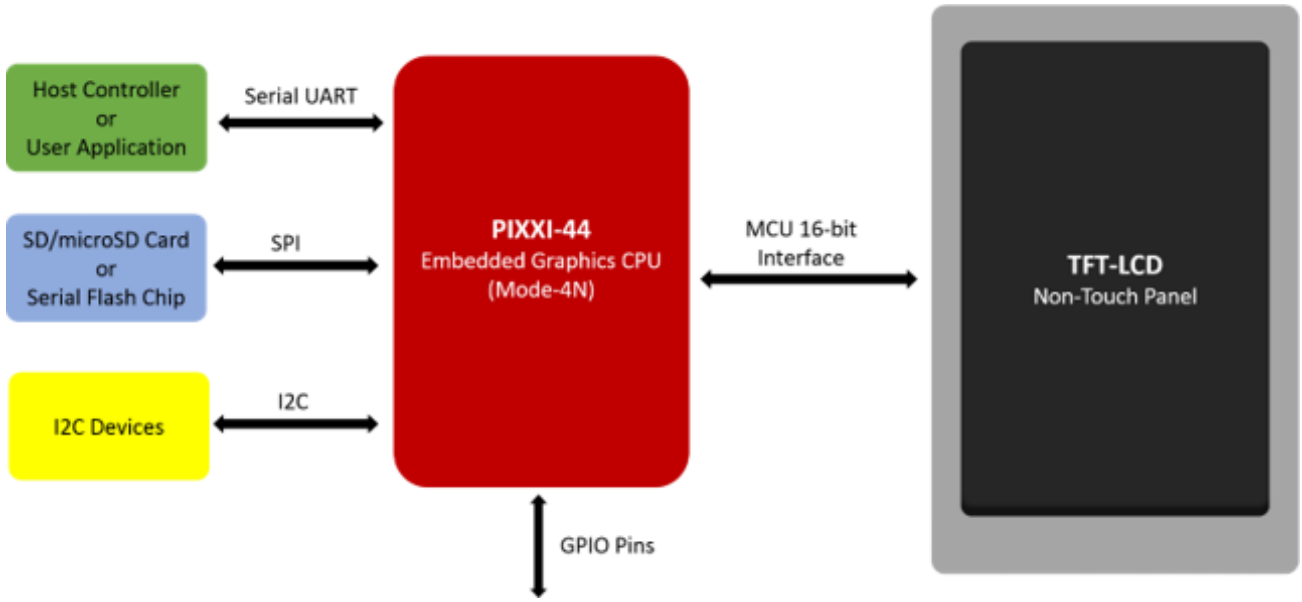
Note

I = Input, **O** = Output, **P** = Power, **A** = Analogue

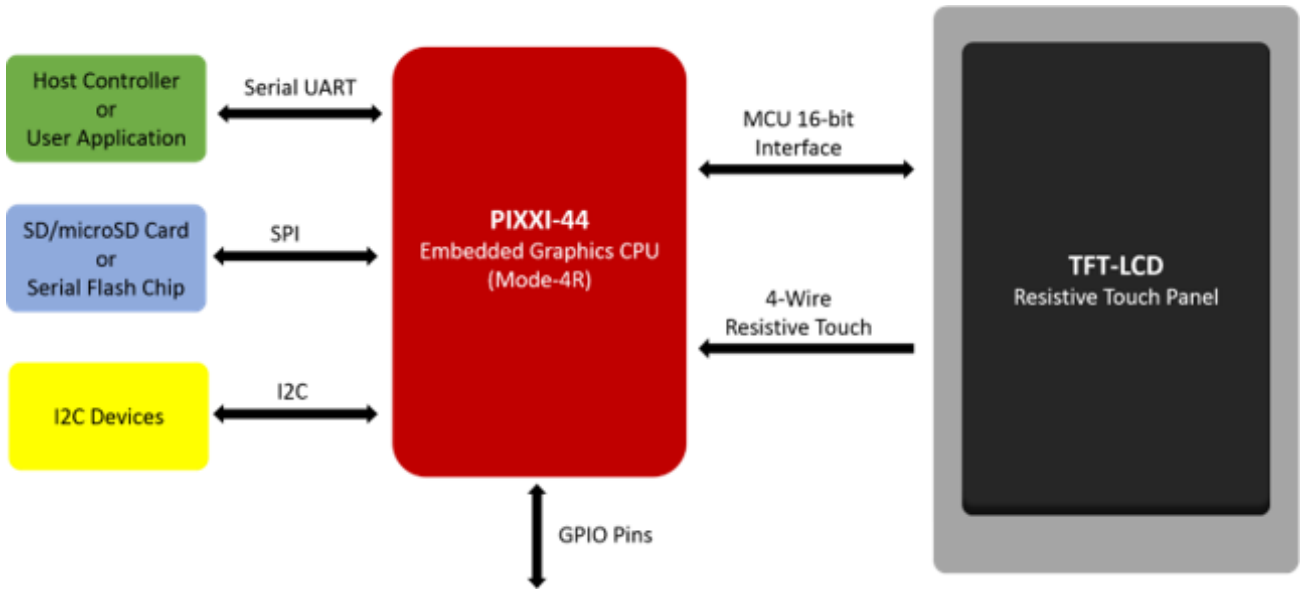
6.4. Mode-4: MCU 16-bit Display Interface

6.4.1. Block Diagrams

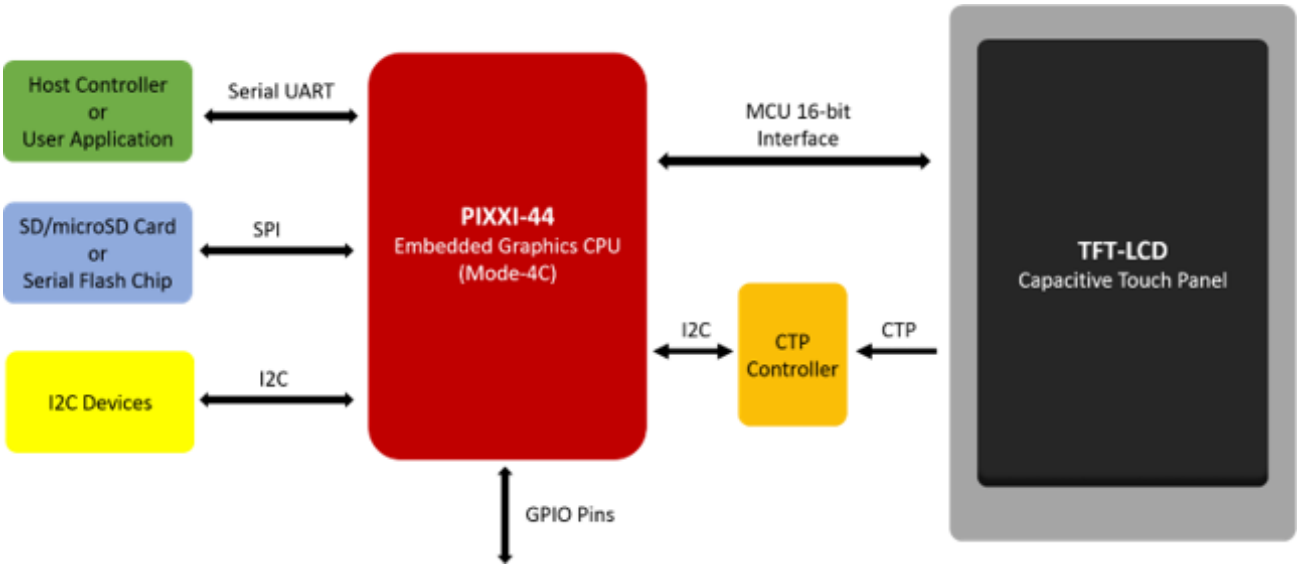
Following block diagrams show the available configurations for different touch panel interfaces under Mode-4.



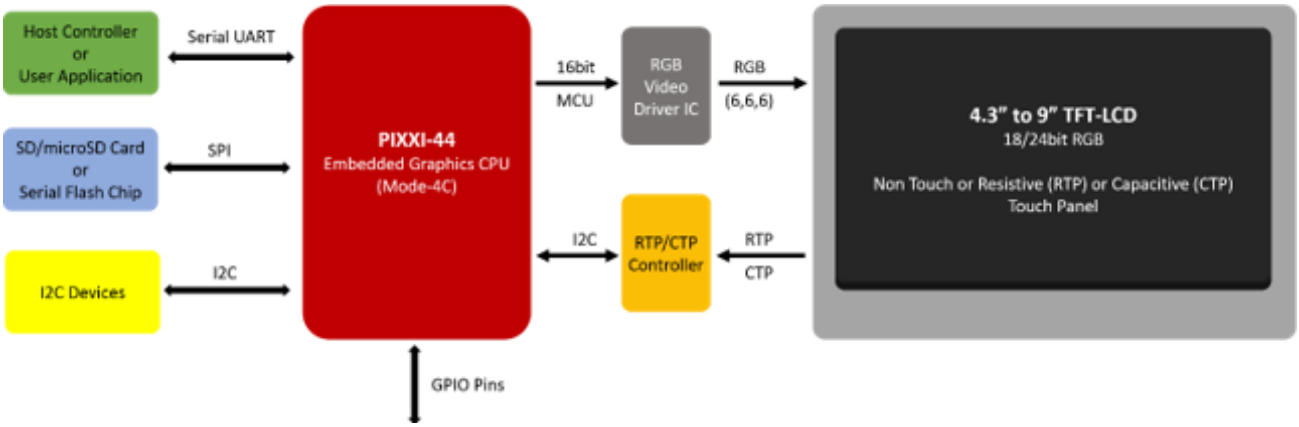
Block Diagram - Mode-4N: MCU 16-bit Display Interface, Non-Touch



Block Diagram - Mode-4R: MCU 16-bit Display Interface, Resistive Touch



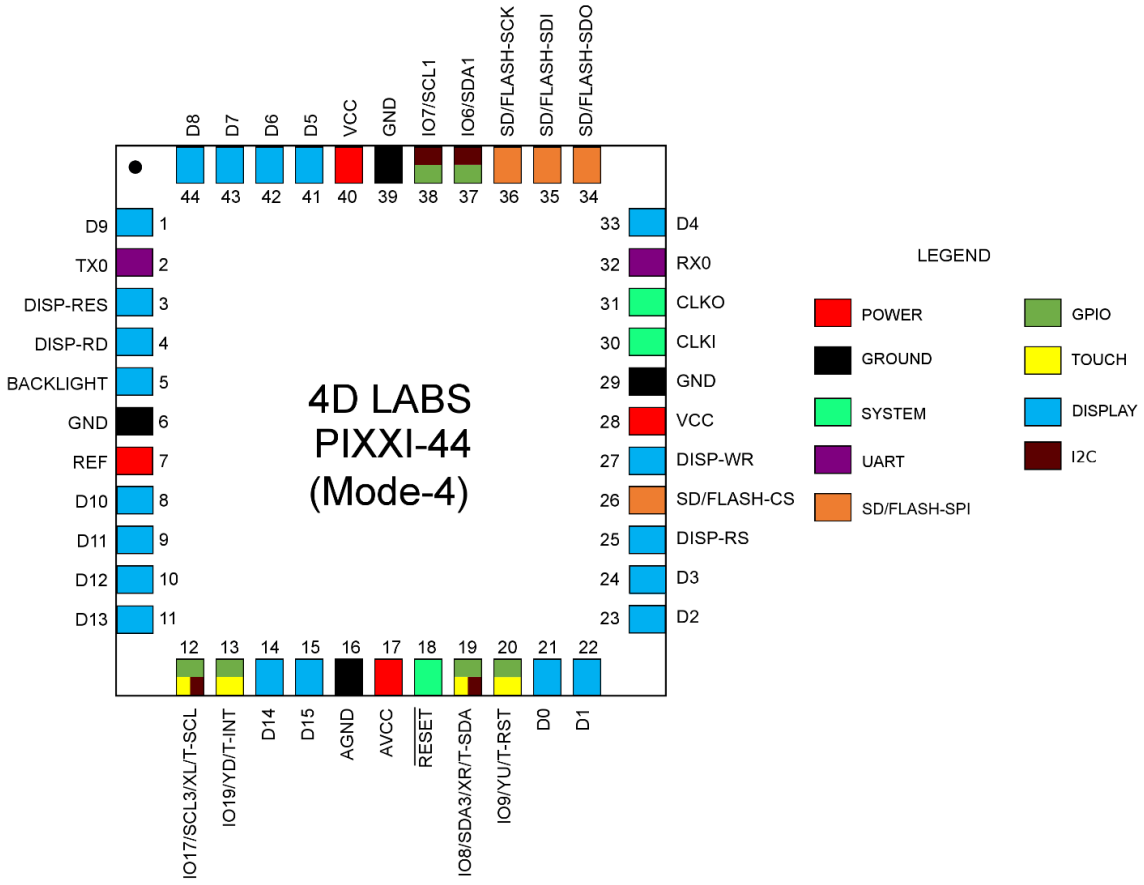
Block Diagram - Mode-4C: MCU 16-bit Display Interface, Capacitive Touch



Block Diagram - Mode-4: RGB 16-bit, NT/RTP/CTP Configuration

6.4.2. Pin Configuration and Summary

The diagram and table below show the pinout diagram and pin descriptions for Mode-4.



Mode-4 Pinout Diagram

Mode-4 Pinout Description

Pin	Symbol	I/O	Description
1	D9	I/O	This pin is Display Data Bus bit 9. This pin outputs 3.3V level and is 5.0V tolerant.
2	TX0	O	Dedicated Asynchronous Serial Port Transmit pin, TX0. This pin outputs 3.3V level.
3	DISP-RES	O	This pin is the Display Reset signal. PIXXI-44 initialises the display by strobing this pin low. Connect this pin to the Reset (RES) signal of the display. This pin outputs 3.3V level.
4	DISP-RD	O	This pin is the Display Read strobe signal. PIXXI-44 asserts this signal low when reading data from the display. Connect this pin to the Read (RD) signal of the display. This pin outputs 3.3V level.
5	BACKLIGHT	O	This pin is the display backlight pin. This pin can output a Pulse Width Modulated (PWM) signal. It can be used with a simple transistor circuit to control backlight LEDs that are in a parallel configuration or it can be used with more complicated DC/DC high voltage circuits for LEDs that have a series configuration. This pin outputs 3.3V level.

Pin	Symbol	I/O	Description
			High: Enable DC-DC converter. Low: Disable DC-DC converter.
6	GND	P	Device Ground.
7	REF	P	Internal voltage regulator filter capacitor pin. Connect a 4.7uF to 10uF capacitor from this pin to Ground. Position capacitor as close as possible.
8	D10	I/O	This pin is Display Data Bus bit 10. This pin outputs 3.3V level and is 5.0V tolerant.
9	D11	I/O	This pin is Display Data Bus bit 11. This pin outputs 3.3V level and is 5.0V tolerant.
10	D12	I/O	This pin is Display Data Bus bit 12. This pin outputs 3.3V level and is 5.0V tolerant.
11	D13	I/O	This pin is Display Data Bus bit 13. This pin outputs 3.3V level and is 5.0V tolerant.
12	IO17/SCL3/ XL/T-SCL	I/O	**Mode-4N:** This pin is available as a GPIO pin. It can also be configured as an I2C clock output pin, SCL3. This pin outputs 3.3V level and is 5.0V tolerant. **Mode-4R:** This pin is XL (4-wire resistive touch screen left signal) pin. Connect this pin to XL or X- signal of the touch panel. **Mode-4C:** This pin is T-SCL (I2C Clock Output) pin. Connect this pin to the I2C clock input (SCL) signal of the capacitive touch controller. This pin outputs 3.3V level.
13	IO19/YD/ T-INT	I/O	**Mode-4N:** This pin is available as a GPIO pin. This pin outputs 0V or 3.3V levels and is 5.0V tolerant as an input. **Mode-4R:** This pin is YD (4-wire resistive touch screen bottom signal) pin. Connect this pin to YD or Y- signal of the touch panel. **Mode-4C:** This pin is T-INT (touch interrupt signal) pin. Connect this pin to the interrupt signal pin of the capacitive touch controller. This pin is 5.0V tolerant.
14	D14	I/O	This pin is Display Data Bus bit 14. This pin outputs 3.3V level and is 5.0V tolerant.
15	D15	I/O	This pin is Display Data Bus bit 15. This pin outputs 3.3V level and is 5.0V tolerant.
16	AGND	P	Analog Ground.
17	AVCC	P	Analog Positive Supply.
18	RESET	I	Master Reset signal. This pin is 5.0V tolerant. Connect a 4.7K pull-up resistor from this pin to VCC. Active Low.
19	IO8/SDA3/ XR/T-SDA	A/I/O	**Mode-4N:** This pin is available as a GPIO pin. It can also be configured as an I2C Data In/Out pin, SDA3. This pin outputs 3.3V level and is 3.3V tolerant only. **Mode-4R:** This pin is XR (4-wire resistive touch screen right signal) pin. Connect this pin to XR or X+ signal of the touch panel. **Mode-4C:** This pin is T-SDA (I2C Data In/Out) pin. Connect this pin to the I2C data in/out signal (SDA) of the capacitive touch controller. This pin outputs 3.3V level and is 3.3V tolerant only.
20	IO9/YU/ T-RST	A/I/O	**Mode-4N:** This pin is available as a GPIO pin. This pin outputs 3.3V level and is 3.3V tolerant only. **Mode-4R:** This pin is YU (4-wire resistive touch screen up signal) pin. Connect this pin to YU or Y+ signal of the touch panel. **Mode-4C:** This pin is T-RST (Touch Reset) pin. Connect this pin to the reset signal of the capacitive touch controller. This pin outputs 3.3V level.
21	D0	I/O	This pin is Display Data Bus bit 0. This pin outputs 3.3V level and is 3.3V tolerant only.
22	D1	I/O	This pin is Display Data Bus bit 1. This pin outputs 3.3V level and is 3.3V tolerant only.
23	D2	I/O	This pin is Display Data Bus bit 2. This pin outputs 3.3V level and is 3.3V tolerant only.
24	D3	I/O	This pin is Display Data Bus bit 3. This pin outputs 3.3V level and is 3.3V tolerant only.
25	DISP-RS	O	This pin is the Display Register Select signal. Connect this pin to the Register Select (RS or A0 or C/D or similar naming convention) signal of the display. This pin outputs 3.3V level.

Pin	Symbol	I/O	Description
			LOW: Display index or status register is selected. HIGH: Display GRAM or register data is selected.
26	SD/ FLASH-CS	O	SD/FLASH SPI Serial Chip Select. SD memory card or serial flash memory chip use only. Connect this pin to the SPI Chip Select (CS) signal of the memory device. This pin outputs 3.3V level.
27	DISP-WR	O	This pin is the Display Write strobe signal. PIXXI-44 asserts this signal low when writing data to the display. Connect this pin to the Write (WR) signal of the display. This pin outputs 3.3V level.
28	VCC	P	Device Positive Supply.
29	GND	P	Device Ground.
30	CLKI	I	Device Clock input 1 of a 12MHz crystal.
31	CLKO	O	Device Clock input 2 of a 12MHz crystal.
32	RX0	I	Dedicated Asynchronous Serial Port Receive pin, RX0. This pin is 5.0V tolerant.
33	D4	I/O	This pin is Display Data Bus bit 4. This pin outputs 3.3V level and is 5.0V tolerant.
34	SD/ FLASH-SDO	O	SD/FLASH SPI Serial Data Output. SD memory card or serial flash memory chip use only. Connect this pin to the SPI Serial Data In (SDI) signal of the memory device. This pin outputs 3.3V level.
35	SD/ FLASH-SDI	I	SD/FLASH SPI Serial Data Input. SD memory card or serial flash memory chip use only. Connect this pin to the SPI Serial Data Out (SDO) signal of the memory device. This pin is 3.3V tolerant.
36	SD/ FLASH-SCK	O	SD/FLASH SPI Serial Clock output. SD memory card or serial flash memory chip use only. Connect this pin to the SPI Serial Clock (SCK) signal of the memory device. This pin outputs 3.3V level.
37	IO6/SDA1	I/O	This pin is available as a General Purpose I/O pin. It can also be configured as an I2C Data In/Out pin, SDA1. This pin outputs 3.3V level and is 3.3V tolerant.
38	IO7/SCL1	I/O	This pin is available as a General Purpose I/O pin. It can also be configured as an I2C clock output pin, SCL1. This pin outputs 3.3V level and is 3.3V tolerant.
39	GND	P	Device Ground.
40	VCC	P	Device Positive Supply.
41	D5	I/O	This pin is Display Data Bus bit 5. This pin outputs 3.3V level and is 5.0V tolerant.
42	D6	I/O	This pin is Display Data Bus bit 6. This pin outputs 3.3V level and is 5.0V tolerant.
43	D7	I/O	This pin is Display Data Bus bit 7. This pin outputs 3.3V level and is 3.3V tolerant only.
44	D8	I/O	This pin is Display Data Bus bit 8. This pin outputs 3.3V level and is 3.3V tolerant only.

Note

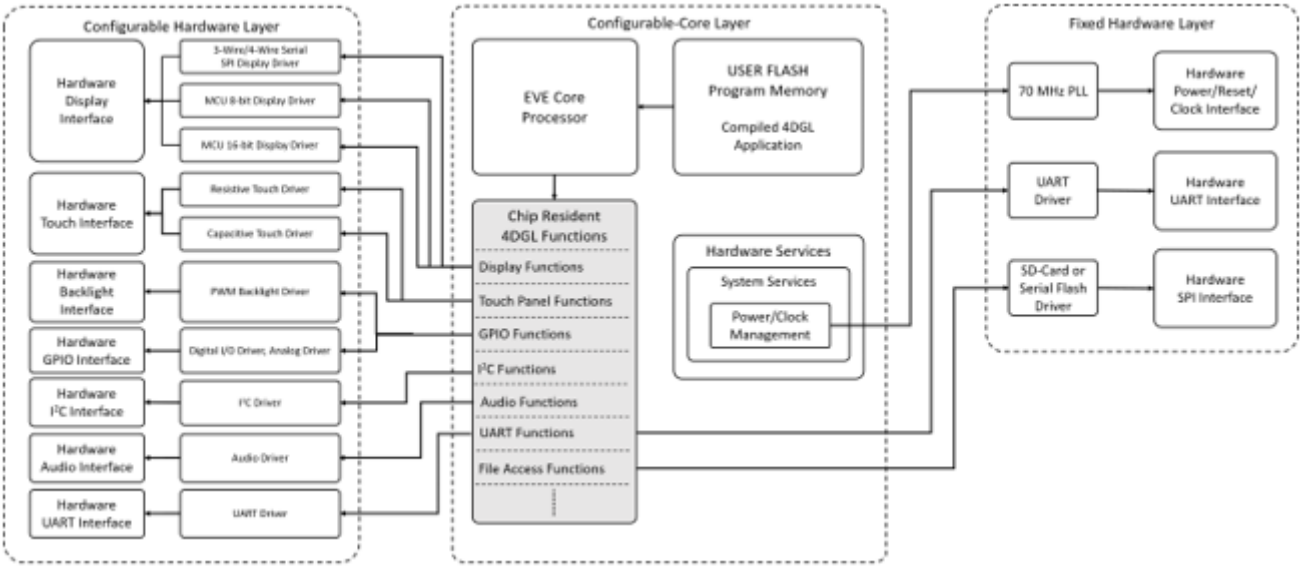
I = Input, **O** = Output, **P** = Power, **A** = Analogue

7. Device Overview

PIXXI-44 belongs to a family of highly optimised and configurable graphics processors. The unique architecture is a combination of physical hardware layers (configurable and fixed) and a soft configurable core layer that seamlessly interact to provide a complete System on a Chip (SoC). There are three main blocks of layers within the device:

- Configurable-Core Layer
- Configurable Hardware Layer
- Fixed Hardware Layer

The figure below presents an overview summary of the interaction between the Hardware and the Configurable-Core layers.



Hardware and Configurable-Core Layers Interaction

There is a direct correlation between the hardware and the configurable core layers and there is no low-level access to any of the hardware peripherals directly. All of the access to the hardware is made available through high level 4DGL functions that reside inside the device, via compiled 4DGL application code. This is described in more detail in the following sections.

The custom display configuration process involves selecting the display interface and touch interface types and setting parameters for the target LCD driver and touch panel using the 4D Labs Project editor in Workshop4 IDE. Workshop4 then automatically generates a corresponding display definition to be used along with a specified PmmC file, which contains the low-level micro-code information of the configurable core and hardware layers. For more details pertaining to custom display configuration, please refer to the **Pixxi Custom Display Configuration User Manual**.

7.1. Configurable-Core Layer

This section describes the configurable core layer of the chip. This layer is a fully configurable soft-core architecture that is designed to speed up application development without the low-level complexities present in other hardware-based architectures. All functionality including the system processor (EVE), the high-level commands as well as the built-in functions are contained in this layer. The configurable layer is defined by the "Personality module micro Code" (PmmC), which is a programmable configuration file. The PmmC file contains all of the low-level micro-code information of the configurable layer, analogy to that of a soft silicon, which define the characteristics and functionality of the device. The ability of programming the device with a PmmC file provides an extremely flexible method of customising as well as upgrading it with future enhancements.

The Configurable-Core layer comprises of three high level sub-blocks ***(EVE Core Block, 4DGL Functions Block, Hardware Services Block)*** and each are described in the following sections.

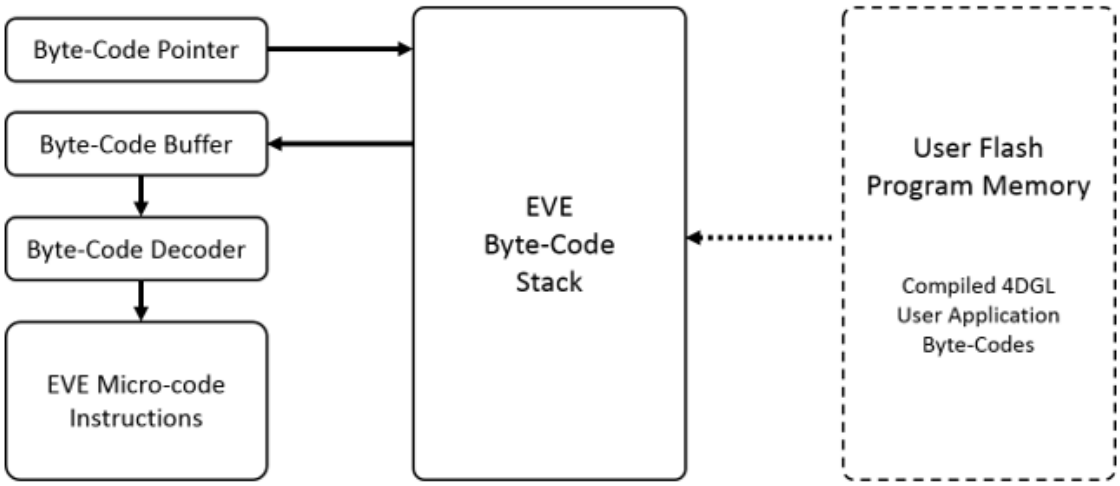
7.1.1. EVE Core Block

EVE (Extensible Virtual Engine) is the heart of the overall system and it's a highly optimised soft-core engine. EVE is a proprietary, high performance processor with an extensive byte-code instruction set optimised to execute compiled 4DGL programs. It is not a conventional microcontroller architecture and therefore low-level access to the chip is not required nor available to the User.

4DGL provides high level functions for the User and does all the low-level work in the background in a highly optimised fashion. 4DGL (4D Graphics Language) was specifically developed from ground up for the EVE engine core. It is a high-level language which is easy to learn and simple to understand yet powerful enough to tackle many embedded graphics applications.

7.1.1.1. EVE State Machine

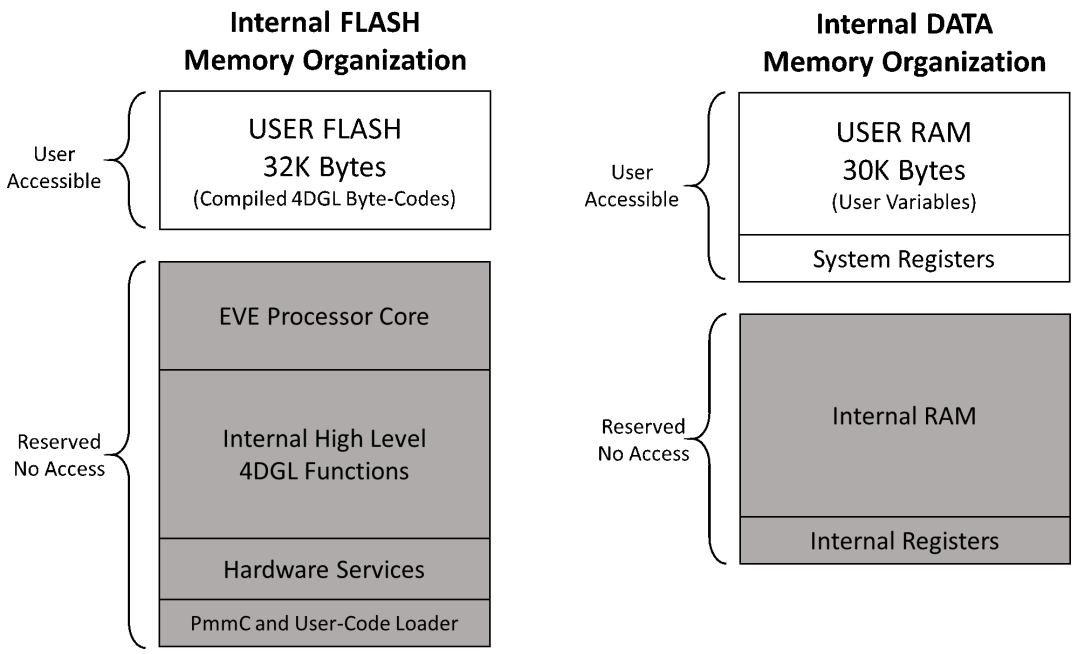
The following diagram gives a brief overview on the working mechanics of the state machine. The Stack is constantly filled with byte codes coming in from the program flash. The byte-code pointer references the next instruction to fetch which then gets decoded and executed. Due to the nature of the high-level design of the configurable core, there is no user access to the state machine, hence there are no assembler type low level op-code instructions. All of the bytecodes are generated by the 4DGL compiler for the user application code.



EVE Core State Machine

7.1.1.2. Memory Organisation and Management

The PIXXI-44 architecture features separate program and data memory spaces and addresses. The figure below illustrates how the internal FLASH and RAM are organised in the device, and what is used by the Virtual System (not user accessible) and what is available for the user.



Device Memory Organisation

User FLASH:

32K bytes of flash memory is available for user application code. The bytecodes in this area are the compiled output from the 4DGL Compiler. The 4DGL Compiler and the chip programming utility programs are available in Workshop4 Software tool (available as a free download).

User RAM:

The PIXXI-44 processor has two banks of RAM, one is 30K bytes of User RAM, and the other is a smaller bank of System RAM which is only usable by the system, for its internal processes. The System RAM is reserved for the system and is not accessible by the user. It is used for processes such as Intermediate File Buffers, Graphics Rendering, etc. This RAM ensures the users RAM is not taken by the system.

No matter what options are enabled by the system, it will never run out of RAM and try to encroach into the user's RAM space. The 30K bytes of User RAM is for storing variables, applications and sub programs etc. Sub programs and Functions stored in RAM can be released when no longer required, freeing the memory for the user.

The user has full access to this 30K bytes of User RAM, and all internal processes of the PIXXI-44 utilise only the separate System RAM.

System Registers:

The PIXXI has a set of System Registers that serve a special purpose. The registers can be directly accessed by using peekW() and pokeW() commands. Accessing these registers are only useful when normal 4DGL functions don't provide enough control over the desired action. For a more detailed description and usage of these registers, please refer to the PIXXI Internal Functions Reference Manual.

The following table outlines in detail the device system registers.

PIXXI System Registers

REGISTER LABEL	USAGE
RANDOM_LO	Random Number Generator Low-Word
RANDOM_HI	Random Number Generator High-Word
SYSTEM_TIMER_LO	1ms System Timer Low-Word
SYSTEM_TIMER_HI	1ms System Timer High-Word
TIMER0	1ms User Timer 0
TIMER1	1ms User Timer 1
TIMER2	1ms User Timer 2
TIMER3	1ms User Timer 3
TIMER4	1ms User Timer 4
TIMER5	1ms User Timer 5
TIMER6	1ms User Timer 6
SYS_X_MAX	display hardware X resolution - 1
SYS_Y_MAX	display hardware Y resolution - 1
GFX_XMAX	width of current orientation
GFX_YMAX	height of current orientation
GFX_LEFT	image left real point
GFX_TOP	image top real point
GFX_RIGHT	image right real point
GFX_BOTTOM	image bottom real point
GFX_X1	image left clipped point
GFX_Y1	image top clipped point
GFX_X2	image right clipped point
GFX_Y2	image bottom clipped point
GFX_X_ORG	current X origin
GFX_Y_ORG	current Y origin
GFX_HILITE_LINE	current multi line button hilite line
GFX_LINE_COUNT	count of lines in multiline button
GFX_LAST_SELECTION	last selected line
GFX_HILIGHT_BACKGROUND	multi button hilite background colour
GFX_HILIGHT_FOREGROUND	multi button hilite background colour
GFX_BUTTON_FOREGROUND	store default text colour for hilite line tracker

REGISTER LABEL	USAGE
GFX_BUTTON_BACKGROUND	store default button colour for hilite line tracker
GFX_BUTTON_MODE	store current buttons mode
GFX_TOOLBAR_HEIGHT	height above
GFX_STATUSBAR_HEIGHT	height below
GFX_LEFT_GUTTER_WIDTH	width to left
GFX_RIGHT_GUTTER_WIDTH	width to right
GFX_PIXEL_SHIFT	pixel shift for button depress illusion
GFX_VECT_X1	gp rect, used by multiline button to hilite required line
GFX_VECT_Y1	
GFX_VECT_X2	
GFX_VECT_Y2	
GFX_THUMB_PERCENT	size of slider thumb as percentage
GFX_THUMB_BORDER_DARK	darker shadow of thumb
GFX_THUMB_BORDER_LIGHT	lighter shadow of thumb
TOUCH_XMINCAL	touch calibration value
TOUCH_YMINCAL	touch calibration value
TOUCH_XMAXCAL	touch calibration value
TOUCH_YMAXCAL	touch calibration value
IMG_WIDTH	width of currently loaded image
IMG_HEIGHT	height of currently loaded image
IMG_FRAME_DELAY	if image, else inter frame delay for movie
IMG_FLAGS	bit 4 determines colour mode, other bits reserved
IMG_FRAME_COUNT	count of frames in a movie
IMG_PIXEL_COUNT_LO	count of pixels in the current frame
IMG_PIXEL_COUNT_HI	count of pixels in the current frame
IMG_CURRENT_FRAME	last frame shown
MEDIA_ADDRESS_LO	micro-SD byte address LO
MEDIA_ADDRESS_HI	micro-SD byte address HI
MEDIA_SECTOR_LO	micro-SD sector address LO
MEDIA_SECTOR_HI	micro-SD sector address HI
MEDIA_SECTOR_COUNT	micro-SD number of bytes remaining in sector
TEXT_XPOS	text current x pixel position
TEXT_YPOS	text current y pixel position
TEXT_MARGIN	text left pixel pos for carriage return
TXT_FONT_TYPE	font type, 0 = system font, else pointer to user font
TXT_FONT_MAX	max number of chars in font
TXT_FONT_OFFSET	starting offset (normally 0x20)
TXT_FONT_WIDTH	current font width
TXT_FONT_HEIGHT	current font height
GFX_TOUCH_REGION_X1	touch capture region

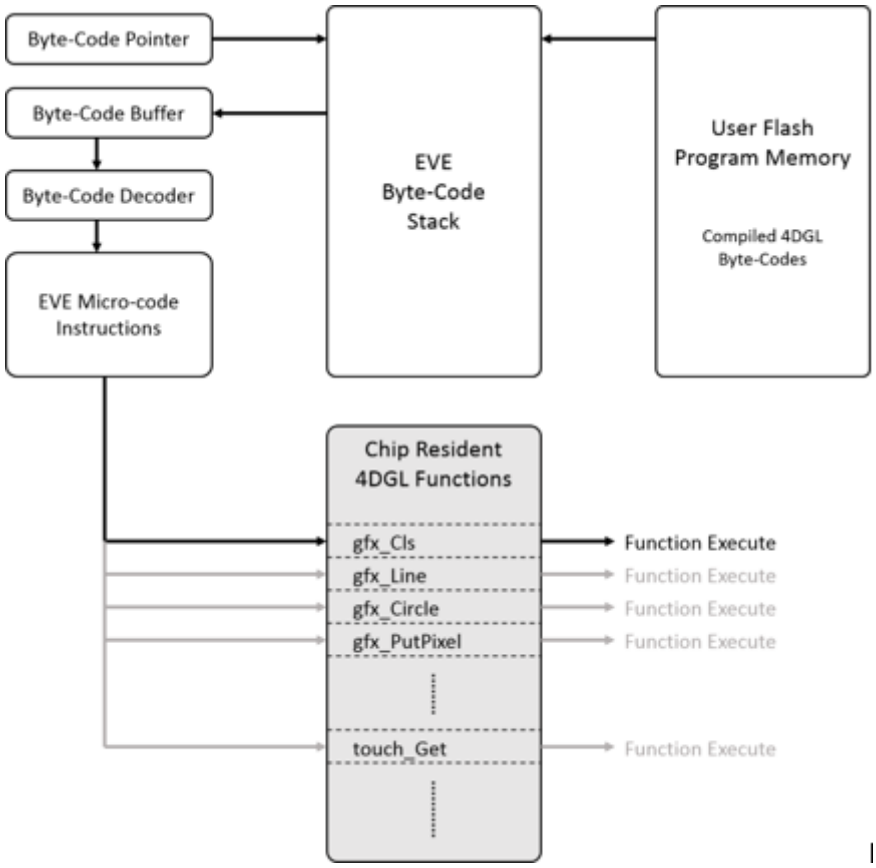
REGISTER LABEL	USAGE
GFX_TOUCH_REGION_Y1	touch capture region
GFX_TOUCH_REGION_X2	touch capture region
GFX_TOUCH_REGION_Y2	touch capture region
GFX_CLIP_LEFT_VAL	left clipping point (set with gfx_ClipWindow(...))
GFX_CLIP_TOP_VAL	top clipping point (set with gfx_ClipWindow(...))
GFX_CLIP_RIGHT_VAL	right clipping point (set with gfx_ClipWindow(...))
GFX_CLIP_BOTTOM_VAL	bottom clipping point (set with gfx_ClipWindow(...))
GFX_CLIP_LEFT	current clip value (reads full size if clipping turned off)
GFX_CLIP_TOP	current clip value (reads full size if clipping turned off)
GFX_CLIP_RIGHT	current clip value (reads full size if clipping turned off)
GFX_CLIP_BOTTOM	current clip value (reads full size if clipping turned off)
GRAM_PIXEL_COUNT_LO	LO word of count of pixels in the set GRAM area
GRAM_PIXEL_COUNT_HI	HI word of count of pixels in the set GRAM area

7.1.2. 4DGL Functions Block

As mentioned in the previous sections, EVE executes bytecodes from compiled 4DGL application programs. 4DGL is a graphics-oriented language allowing rapid application development. An extensive library of graphics, text, file system and many other functions are implemented inside chip. The built-in library and the ease of use of the language that combines the best elements and syntax structure of languages such as C, Basic, Pascal, etc.

Programmers familiar with these languages will feel right at home with 4DGL. It includes many familiar instructions such as; ***If..Else..Endif, While..Wend, Repeat..Until, Gosub..Endsub, Goto*** as well as a wealth of (chip-resident) internal functions that include ***serin, serout, gfx_Line, gfx_Circle*** and many more.

The diagram below is an overview on the workings of these built-in functions.



Built-in 4DGL Functions Structure

The list below summarizes the built-in 4DGL functions residing inside the PIXXI. For a more detailed description and usage of these functions, please refer to the PIXXI Internal Functions Reference Manual.

- Graphics Functions
- Touch Screen Functions
- System Memory Access Functions
- Maths Functions
- Text and String Functions
- Display Access Functions
- Media Functions (SD/SDHC Memory Card or Serial Flash Chip)
- Serial (UART) Communications Functions
- I2C BUS Master Functions
- Timer Functions
- FAT16 File Functions
- General Purpose Functions
- String Class Functions
- Image Control Functions
- Memory Allocation Functions
- Audio Functions
- Internal Widgets

7.1.3. Hardware Services Block

The Hardware Services block takes care of all the background system processes. The information presented in this section is for providing some overview to the user. All services are background processes and the user have no access to these.

7.1.4. System Services

Internal core-registers, power and clock distribution, PmmC-file and user-code loaders are maintained within this sub-block.

Internal Registers Services:

The PIXXI has a set of Internal Registers that serve a special purpose. The registers can be directly accessed by using peekW() and pokeW() commands.

Power and Clock Management:

Power and clock distribution are managed by this sub-block. The user does not need to have access to the services in this sub-block.

PmmC-File Loader:

PmmC (Personality Module Micro-Code) - this is the configuration file that defines the Configurable-Core Layer. The PmmC-File Loader can be thought of like a bootloader. It allows the transfer of a PmmC file from the user's PC into the system flash storage on the PIXXI processor.

Within the PmmC are over 200 built-in functions for graphics, sound, math functions etc. There is no need to include libraries, or wait for hefty compile times - it's all built in.

The PmmC is in protected memory and cannot be read or damaged by inadvertent writes to illegal FLASH areas.

User-Code Loader:

The user code is the compiled output of the 4DGL compiler. The User-Code Loader allows the transfer of a user code from the user's PC to the system flash storage on the PIXXI processor.

Similar to the PmmC, the user code is in protected memory, and cannot be read or damaged by inadvertent writes to illegal FLASH areas.

7.1.5. TIMER Interrupt Services

Timer interrupt services are maintained within this sub-block.

7.2. Hardware Layer

This section describes the hardware layer of the chip. The PIXXI-44 has the essential hardware peripherals for interfacing with many popular OLED and LCD display panels and touch panels. It also has interfaces for communicating with other external devices through digital input/output, analog input, I2C ports, and UART pins. The following sections explain the features of these hardware peripherals in detail.

7.2.1. Configurable Hardware Layer

This section describes in detail the configurable hardware interface.

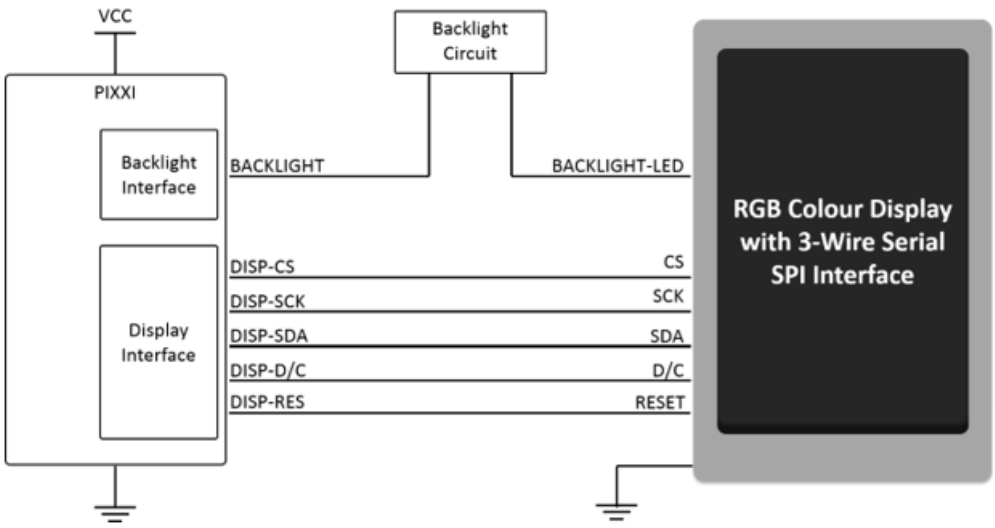
7.2.1.1. Display Interface

As discussed in the section Device Configuration Modes, the PIXXI-44 has four modes of configuration, each of which correspond to a specific display interface. The PIXXI-44 can be configured to support LCD and OLED displays with an SPI interface, either in 3-wire serial SPI configuration (Mode-1) or 4-wire serial SPI configuration (Mode-2). The PIXXI-44 can also be configured to support MCU 8-bit (Mode-3) and MCU 16-bit (Mode-4) display interfaces. Only one mode of configuration at a time is possible. After having been configured for a certain mode, the PIXXI-44 generates all of the necessary timing to drive the display. The connectivity to the display is easy and straight forward. For more details pertaining to custom display configuration, please refer to the **Pixxi Custom Display Configuration User Manual**.

> **Note**
>
> The unique architecture of the device allows rendering of graphics using high-level 4DGL functions. For more information regarding 4DGL functions, please refer to the PIXXI Internal Functions Reference Manual.

Mode-1: 3-Wire Serial SPI Configuration

The figure below shows a typical connection diagram for a display with 3-wire serial SPI interface.



Typical 3-Wire Serial SPI Interface Connection

Display Interface Pins

DISP-RES:

Display RESET signal (active low). This pin is used to reset or enable the display. Connect this pin to the Reset (RESET) signal of the display. [LOW: Display is held in Reset, HIGH: Display is released from Reset and Enabled]

DISP-D/C:

Display Data or Command signal. This pin is used to select command or parameter/display. Connect this pin to the Data or Command selection (D/C) pin of the display. [LOW: Command is selected, HIGH: Parameter or display data is selected]

DISP-CS:

Display Chip Select signal (active low). This pin is used to select the display. Connect this pin to the SPI Chip Select (CS) pin of the display, if needed.

DISP-SDA:

Display SPI Serial Data In/Out signal. Connect this pin to the Serial Data In/Out (SDA) pin of the display.

DISP-SCK:

Display SPI Serial Clock Output signal. Connect this pin to the Serial Clock (SCK) pin of the display.

DISP-BL:

The backlight control pin is a Pulse Width Modulated (PWM) signal. It can be used with a simple transistor circuit to control backlight LEDs that are in a parallel configuration or it can be used with a more complicated DC/DC high voltage circuits for LEDs that have a series configuration. See the Backlight Interface section for more details.

> **Note**
>
> Different displays utilise various pin naming conventions. Be sure to check with your display manufacturer for the correct name and function.

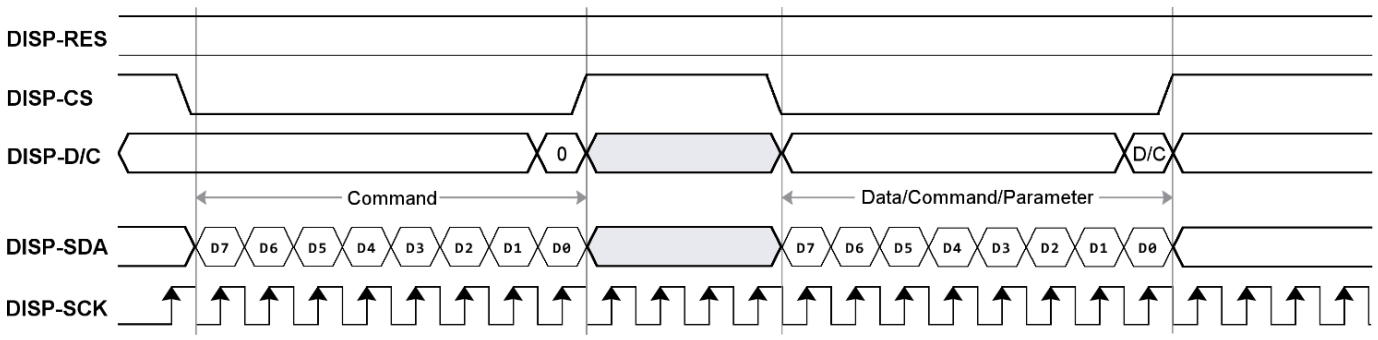
Write Cycle Sequence

In a write cycle, the PIXXI sends a command or data (composed of 8 bits) to the display module through the DISP-SDA line. The diagram below describes a typical write cycle sequence for the 3-wire serial SPI interface.

In the example below, the MSB is transmitted first. Also, the PIXXI sets the data bits on the falling edges of the DISP-SCK signal. The display module, on the other hand, reads the data bits on the rising edges of the DISP-SCK signal.

At the beginning part of the write cycle, PIXXI asserts the DISP-CS signal low to signal the start of data transmission and sets the MSB (D7) on the DISP-SDA line. The display module reads the MSB (D7) on the DISP-SDA line on the first rising edge of DISP-SCK just after DISP-CS is asserted low. PIXXI then sets the next data bit (D6) on the next falling edge of DISP-SCK. Data bit D6 is then read by the display module on the second rising edge of DISP-SCK.

This sequence is repeated until the 7^{th} falling edge on the DISP-SCK line. On the 8^{th} falling edge of DISP-SCK, the PIXXI sets the LSB D0 on the DISP-SDA line and asserts the DISP-D/C high or low, depending on the type (command or parameter/display data) of the data being transmitted.

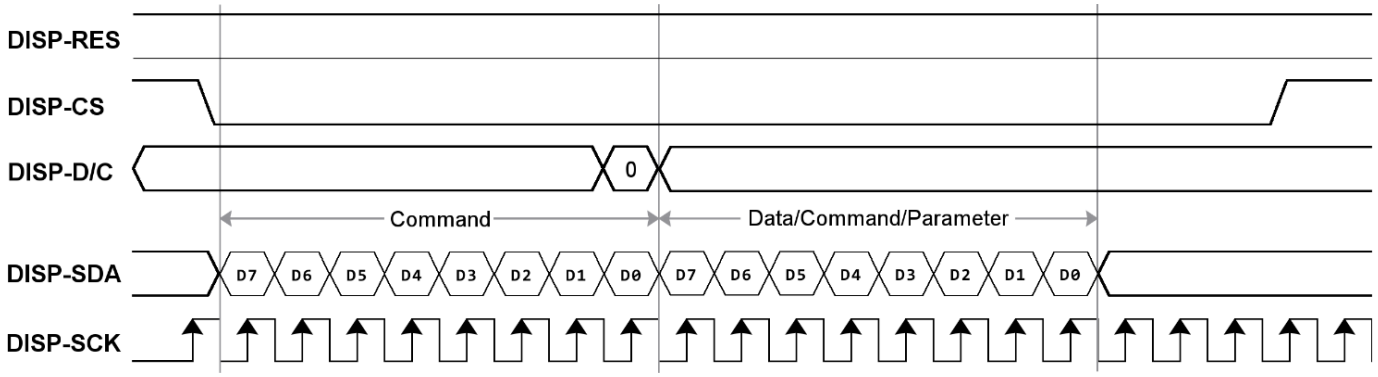


3-Wire Serial SPI Write Cycle Sequence Diagram

In the case of the diagram above, the DISP-D/C line is set low to indicate that the byte being transmitted is a command. A write cycle for a single byte is now complete. A few write cycles might be needed to facilitate the transfer of the whole message. The first byte (command) could be followed by parameter data. Between each write cycle, the DISP-CS signal can be asserted high. Any data on the DISP-SDA line during this time is invalid.

Read Cycle Sequence

In a read cycle, the PIXXI reads a register parameter or display data from the display module through the DISP-SDA line. The diagram below describes a typical read cycle sequence for the 3-wire serial SPI configuration.



3-Wire Serial SPI Read Cycle Sequence Diagram

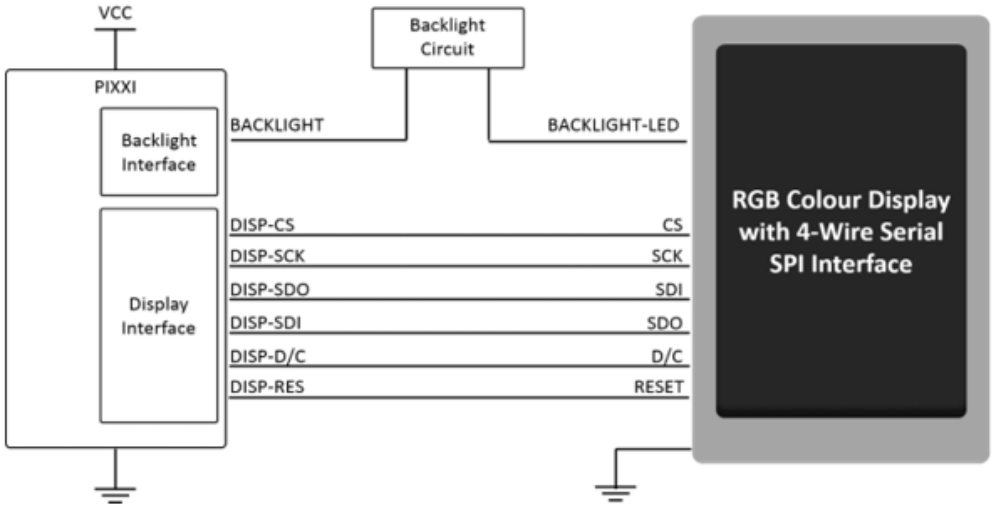
First, the PIXXI has to send a read ID or register command to the display module. After the read command has been sent, the DISP-SDA line must be set to tri-state no later than the falling edge of the DISP-SCK signal at the last bit. The display module then transmits back the parameter or data through the DISP-SDA line. Data bits are latched by the display module on the DISP-SDA line at the rising edges of the DISP-SCK signal and are set at the falling edges of the DISP-SCK signal. The read cycle sequence has three types of transmitted data - 8-bit, 24-bit, and 32-bit.

Timing Characteristics

For information on the typical timing characteristics for the 3-wire and 4-wire serial SPI configurations, refer to the info about the Timing Characteristics under the 4-Wire Serial SPI Configuration.

Mode-2: 4-Wire Serial SPI Configuration

The figure below shows a typical connection diagram for a display with 4-wire serial SPI interface.



Typical 4-Wire Serial SPI Interface Connection

Display Interface Pins

DISP-RES:

Display RESET signal (active low). This pin is used to reset or enable the display. Connect this pin to the Reset (RESET) signal of the display [**LOW**: Display is held in Reset, **HIGH**: Display is released from Reset and Enabled]

DISP-D/C:

Display Data or Command signal. This pin is used to select command or parameter/display. Connect this pin to the Data or Command selection (D/C) pin of the display. [**LOW**: Command is selected, **HIGH**: Parameter or display data is selected]

DISP-CS:

Display Chip Select signal (active low). This pin is used to select the display. Connect this pin to the SPI Chip Select (CS) pin of the display, if needed.

DISP-SDI:

Display SPI Serial Data In signal. Connect this pin to the Serial Data Out (SDO) pin of the display.

DISP-SDO:

Display SPI Serial Data Out signal. Connect this pin to the Serial Data In (SDI) pin of the display.

DISP-SCK:

Display SPI Serial Clock Output signal. Connect this pin to the Serial Clock (SCK) pin of the display.

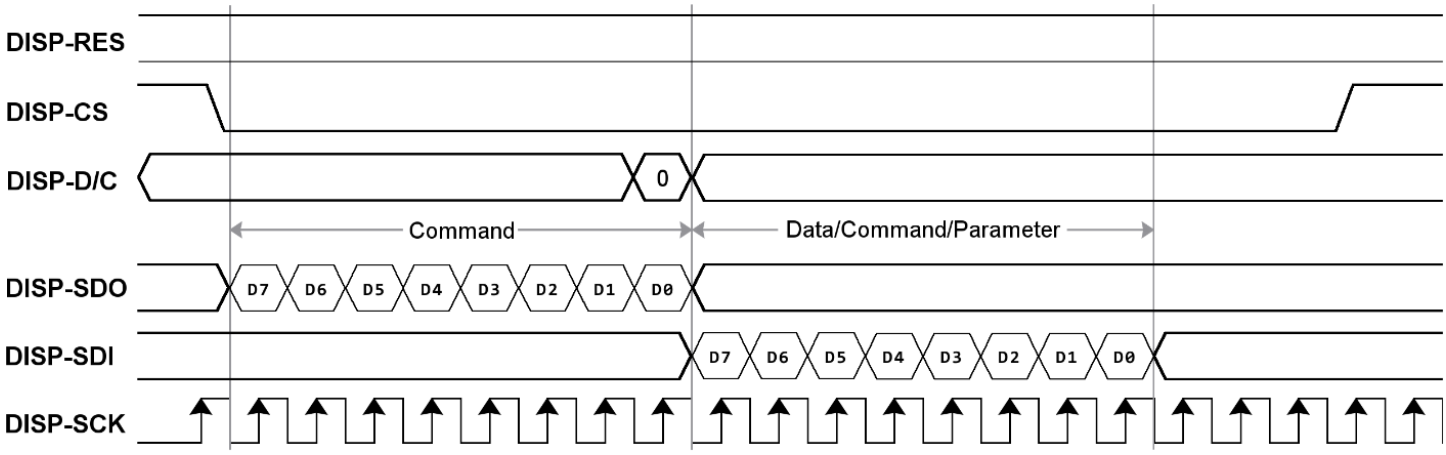
DISP-BL:

The backlight control pin is a Pulse Width Modulated (PWM) signal. It can be used with a simple transistor circuit to control backlight LEDs that are in a parallel configuration or it can be used with a more complicated DC/DC high voltage circuits for LEDs that have a series configuration. See the Backlight Interface section for more details.

> **Note**
>
> Different displays utilise various pin naming conventions. Be sure to check with your display manufacturer for the correct name and function.

Read Cycle Sequence

In a read cycle, the PIXXI reads a register parameter or display data from the display module through the DISP-SDI line. The diagram below describes a typical read cycle sequence for the 4-wire serial SPI configuration.

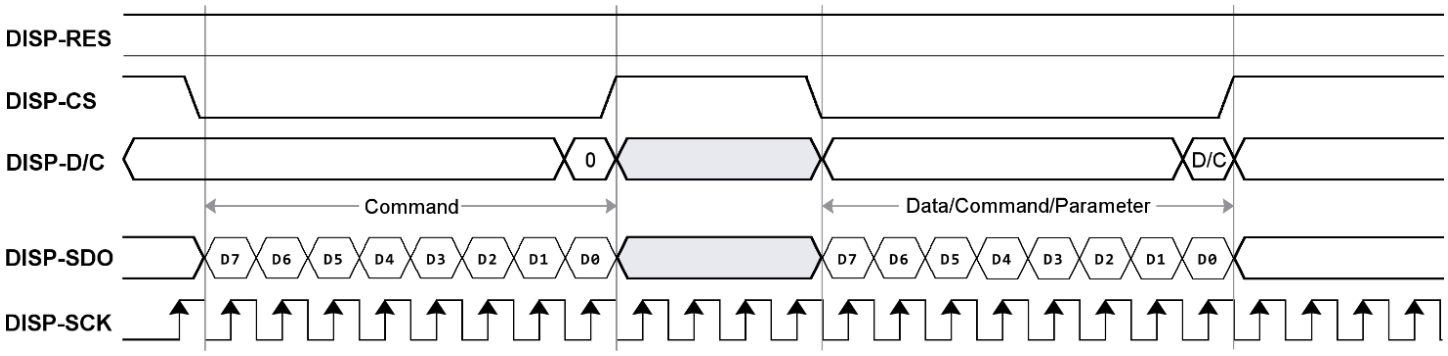


4-Wire Serial SPI Read Cycle Sequence Diagram

First, the PIXXI must send a read ID or register command to the display module through the DISP-SDO line. The display module then transmits back the parameter or data through the DISP-SDI line. Data bits are latched by the display module on the DISP-SDI line at the rising edges of the DISP-SCK signal and are set at the falling edges of the DISP-SCK signal. The read cycle sequence has three types of transmitted data - 8-bit, 24-bit, and 32-bit.

Write Cycle Sequence

In a write cycle, the PIXXI sends a command or data (composed of 8 bits) to the display module through the DISP-SDO line. The diagram below describes a typical write cycle sequence for the 4-wire serial SPI interface. In the example below, the MSB is transmitted first. Also, the PIXXI sets the data bits on the falling edges of the DISP-SCK signal. The display module, on the other hand, reads the data bits on the rising edges of the DISP-SCK signal.



4-Wire Serial SPI Write Cycle Sequence Diagram

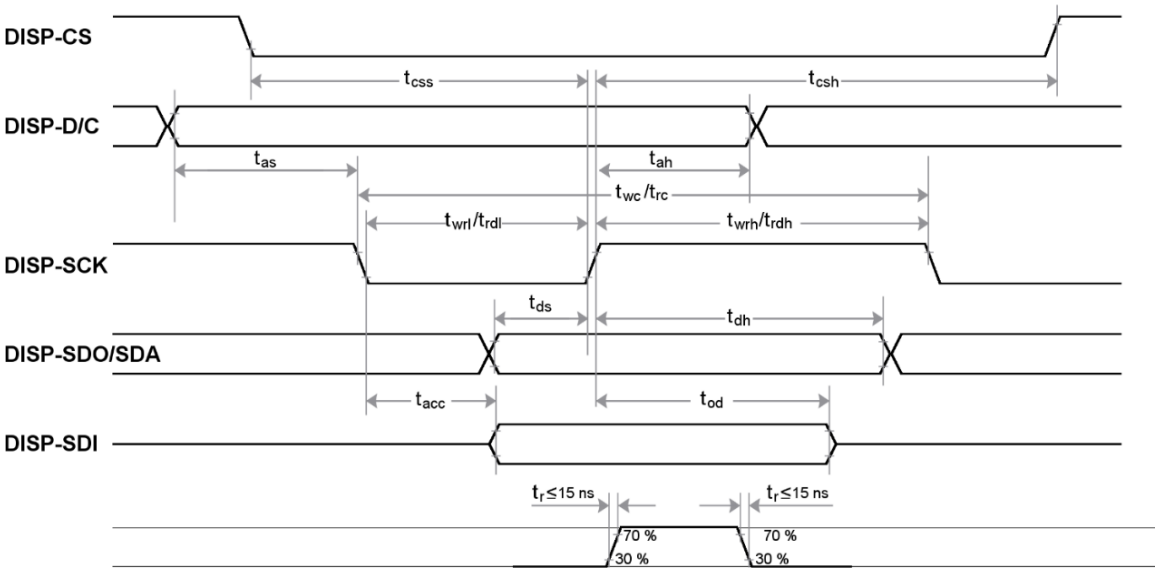
At the beginning part of the write cycle, PIXXI asserts the DISP-CS signal low to signal the start of data transmission and sets the MSB (D7) on the DISP-SDO line. The display module reads the MSB (D7) on the DISP-SDO line on the first rising edge of DISP-SCK just after DISP-CS is asserted low. PIXXI then sets the next data bit (D6) on the next falling edge of DISP-SCK. Data bit D6 is then read by the display module on the second rising edge of DISP-SCK.

This sequence is repeated until the 7^{th} falling edge on the DISP-SCK line. On the 8^{th} falling edge of DISP-SCK, the PIXXI sets the LSB D0 on the DISP-SDO line and asserts the DISP-D/C high or low, depending on the type (command or parameter/display data) of the data being transmitted.

In the case of the previous diagram, the DISP-D/C line is set low to indicate that the byte being transmitted is a command. A write cycle for a single byte is now complete. A few write cycles might be needed to facilitate the transfer of the whole message. The first byte (command) could be followed by parameter data. Between each write cycle, the DISP-CS signal can be asserted high. Any data on the DISP-SDO line during this time is invalid.

Timing Characteristics

The figure and table below show the typical timing characteristics for the 3-wire and 4-wire serial SPI configurations.



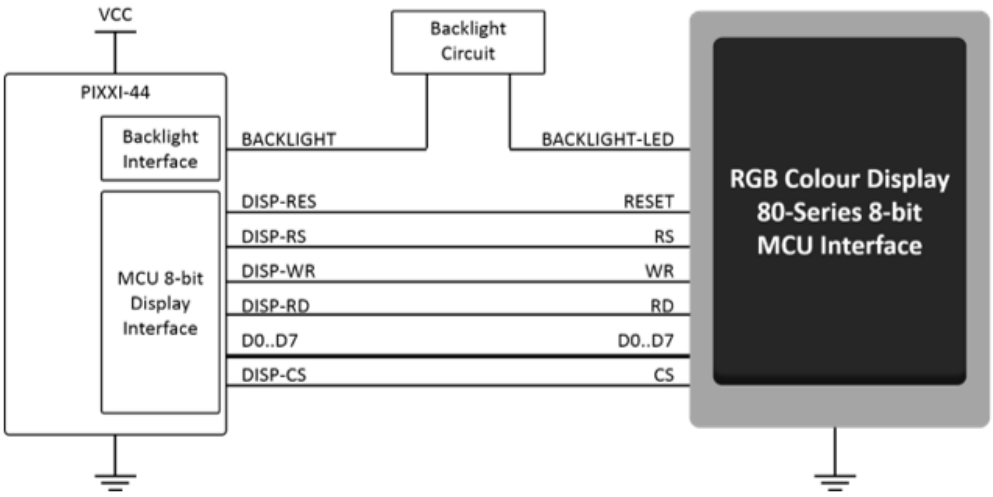
Timing Characteristics for 3-wire and 4-wire Serial SPI Configurations

Timing Values for 3-wire and 4-wire Serial SPI Configurations

SIGNAL	SYMBOL	PARAMETER	MIN	MAX	UNIT	DESCRIPTION
DISP-CS	tcss	Chip select time (Write)	40	-		
	tcsh	Chip select hold time (Read)	40	-	ns	
DISP-SCK	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCK "H" pulse width (Write)	40	-	ns	
	twrl	SCK "L" pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCK "H" pulse width (Read)	60	-	ns	
	trdl	SCK "L" pulse width (Read)	60	-	ns	
DISP-D/C	tas	D/C setup time	10	-	ns	
	tah	D/C hold time (Write/Read)	10	-	ns	
DISP-SDO/SDA	tds	D/C setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
DISP-SDI	tacc	Access time (Read)	10	-	ns	
	tod	Output disable time (Read)	10	50	ns	For maximum CL = 30pF For minimum CL = 8pF

Mode-3: MCU 8-bit Configuration

The figure below shows a typical connection diagram for a display with MCU 8-bit display interface.



Typical MCU 8-bit Interface Connection

Display Interface Pins

D0-D7 Pins:

Display Data Bus. The Display Data Bus (D0-D7) is an 8-bit bidirectional port and all data writes and reads occur over this bus. Other control signals such as DISP-WR, DISP-RD, DISP-CS, and DISP-RS synchronise the data transfer to and from the display.

DISP-RES:

Display RESET signal (active low). This pin is used to reset or enable the display. Connect this pin to the Reset (RESET) signal of the display. [**LOW**: Display is held in Reset, **HIGH**: Display is released from Reset and Enabled]

DISP-D/C:

Display Register Select signal. This determines whether a register command or data is sent to the display. Connect this pin to the Register Select (RS) signal of the display. Different displays utilise various naming conventions such as RS, A0, C/D or similar. Be sure to check with your display manufacturer for the correct name and function. [**LOW**: Display index or status register is selected, **HIGH**: Display GRAM or register data is selected]

DISP-CS:

Display Chip Select signal (active low). This pin is used to select the display. Connect this pin to the Chip Select (CS) pin of the display, if needed.

DISP-WR:

Display Write strobe signal. PIXXI-44 asserts this signal LOW when writing data to the display in conjunction with the display data bus (D0-D7). Connect this pin to the Write (WR) signal of the display.

DISP-RD:

Display Read strobe signal. PIXXI-44 asserts this signal LOW when reading data from the display in conjunction with the display data bus (D0-D7). Connect this pin to the Read (RD) signal of the display.

BACKLIGHT:

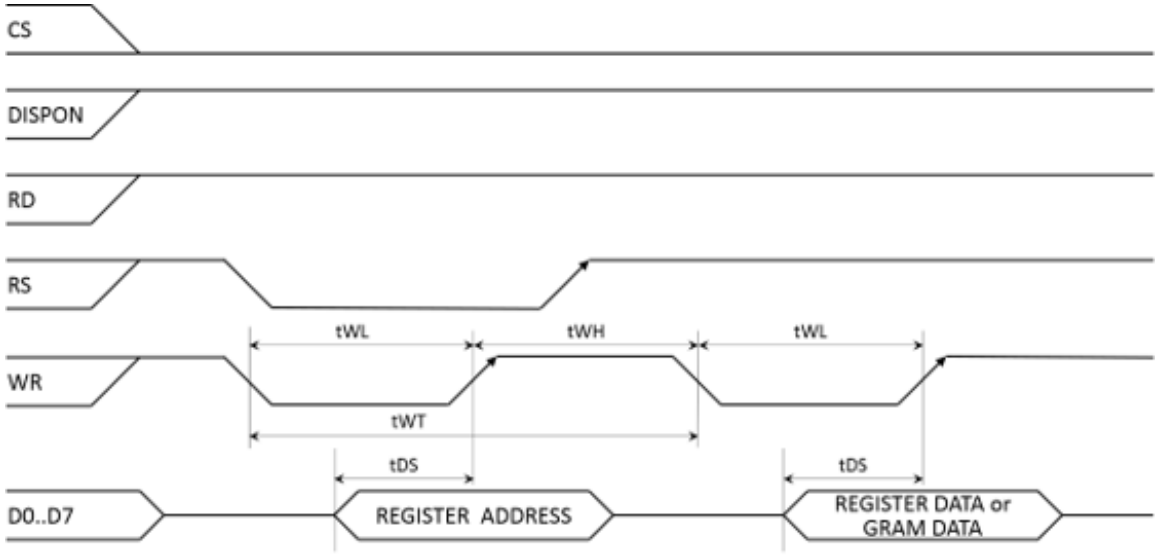
The backlight control pin is a Pulse Width Modulated (PWM) signal. It can be used with a simple transistor circuit to control backlight LEDs that are in a parallel configuration or it can be used with a more complicated DC/DC high voltage circuits for LEDs that have a series configuration. See the Backlight Interface section for more details.

Note

Different displays utilise various pin naming conventions. Be sure to check with your display manufacturer for the correct name and function.

Write Cycle Sequence and Signal Timing

In a write cycle, the PIXXI sends a command or data to the display module through the data bus. The following diagram and table show the write cycle and timing values for the MCU 8-bit interface.



MCU 8-bit Write Cycle Sequence and Signal Timing Diagram

MCU 8-bit Write Signal Timing Values

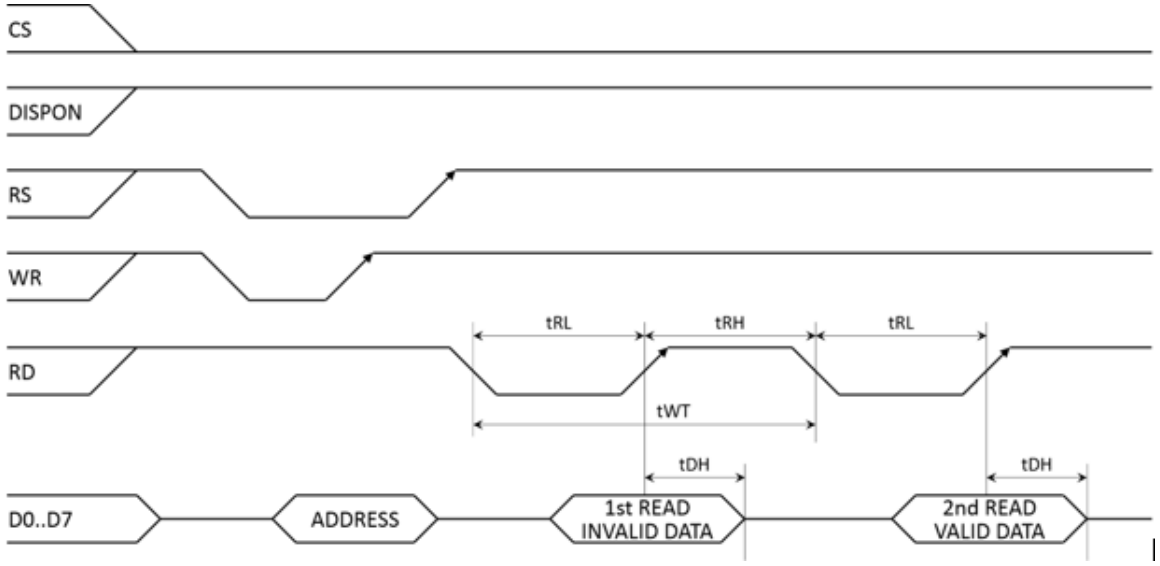
Item	Symbol	Min	Typ	Max	Unit
Write Low Pulse	tWL	50	-	-	ns
Write High Pulse	tWH	50	-	-	ns
Write Bus Cycle Total	tWT	100	-	-	ns
Write Data Setup	tDS	25	-	-	ns

In a write cycle sequence, the DISP-WR signal is driven from HIGH to LOW and then pulled back to HIGH. The display module captures the information from the data bus on the rising edge of DISP-WR. During this time, if the DISP-RS signal is driven to a low level, the display interprets the data on the display bus as command/register address information. If the DISP-RS signal is pulled up high, the display interprets the data as command/register parameter information or as GRAM pixel data.

The process described above is fully automated and the designer need not have to worry about the working mechanics. This is one of the plug-and-play features of the chip. The designer just needs to make the right signal connections.

Read Cycle Sequence and Signal Timing

In a read cycle, the PIXXI reads a command or data from the display module through the data bus. The following diagram and table show the read cycle and timing values for the MCU 8-bit interface.



MCU 8-bit Read Cycle Sequence and Signal Timing Diagram

MCU 8-bit Read Signal Timing Values

Item	Symbol	Min	Typ	Max	Unit
Read Low Pulse	tRL	150	-	-	ns
Read High Pulse	tRH	150	-	-	ns
Read Bus Cycle Total	tRT	300	-	-	ns
Read Data Setup	tDH	75	-	-	ns

The read cycle is a 2-phase process.

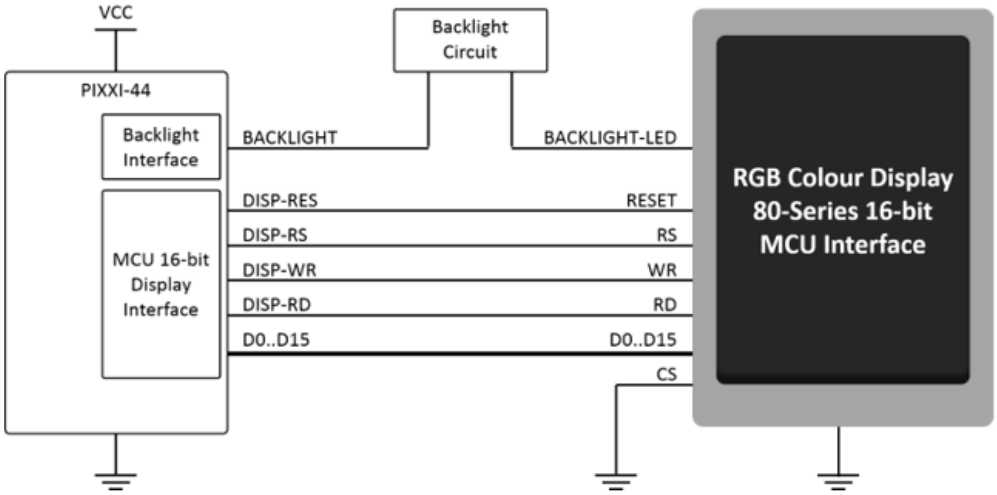
Phase 1: Before the desired display data is read, PIXXI must first select the register or the GRAM address location. It does this by performing a write cycle operation of the location.

Phase 2: PIXXI then asserts the DISP-RD signal by driving it from HIGH to LOW and then pulling it back to HIGH during the read cycle. The display module provides the information to the bus during the read cycle on the rising edge of DISP-RD signal.

The process described above is fully automated and the designer need not have to worry about the working mechanics. This is one of the plug-and-play features of the chip. The designer just needs to make the right signal connections.

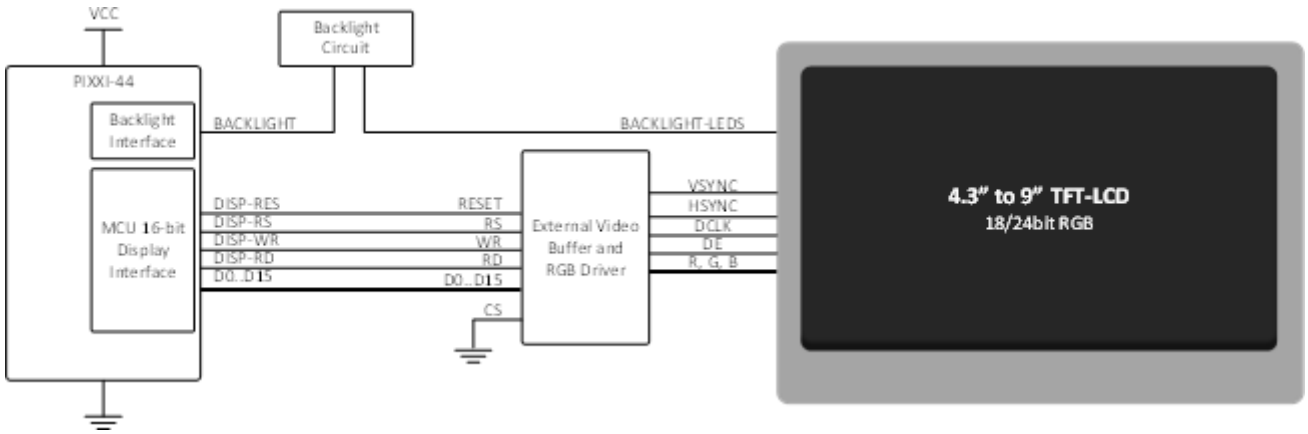
Mode-4: MCU 16-bit Configuration

The figure below shows a typical connection diagram for a display with MCU 16-bit display interface.



Typical MCU 16-bit Interface Connection

The PIXXI-44 can also be interfaced to RGB displays using an external video buffer and RGB driver IC, as shown below.



Typical RGB 16-bit Interface Connection using an RGB Video Driver IC

Display Interface Pins

D0-D15 Pins:

Display Data Bus. The Display Data Bus (D0-D15) is a 16-bit bidirectional port and all data writes and reads occur over this bus. Other control signals such as DISP-WR, DISP-RD, DISP-CS, and DISP-RS synchronise the data transfer to and from the display.

DISP-RES:

Display RESET signal (active low). This pin is used to reset or enable the display. Connect this pin to the Reset (RESET) signal of the display. [**LOW**: Display is held in Reset, **HIGH**: Display is released from Reset and Enabled]

DISP-RS:

Display Register Select signal. This determines whether a register command or data is sent to the display. Connect this pin to the Register Select (RS) signal of the display. Different displays utilise various naming conventions such as RS, A0, C/D or similar. Be sure to check with your display manufacturer for the correct name and function. [**LOW**: Display index or status register is selected, **HIGH**: Display GRAM or register data is selected]

DISP-CS:

Display Chip Select signal (active low). This pin is used to select the display. Connect this pin to the Chip Select (CS) pin of the display, if needed.

DISP-WR:

Display Write strobe signal. PIXXI-44 asserts this signal LOW when writing data to the display in conjunction with the display data bus (D0-D15). Connect this pin to the Write (WR) signal of the display.

DISP-RD:

Display Read strobe signal. PIXXI-44 asserts this signal LOW when reading data from the display in conjunction with the display data bus (D0-D15). Connect this pin to the Read (RD) signal of the display.

BACKLIGHT:

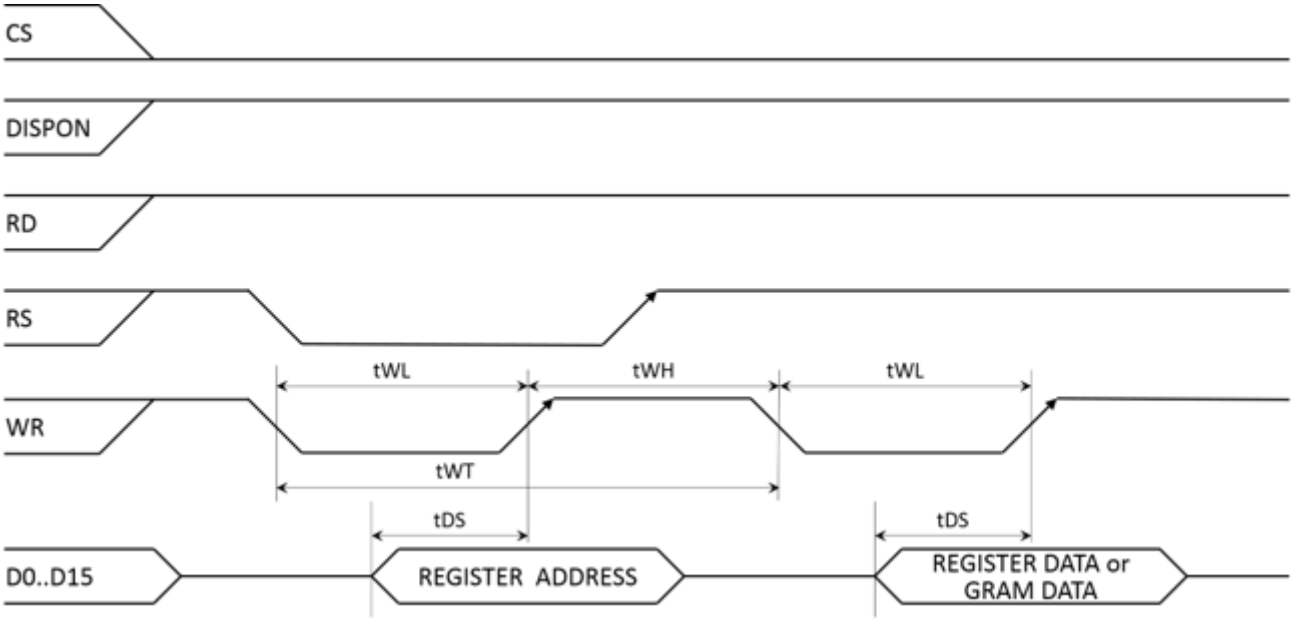
The backlight control pin is a Pulse Width Modulated (PWM) signal. It can be used with a simple transistor circuit to control backlight LEDs that are in a parallel configuration or it can be used with a more complicated DC/DC high voltage circuits for LEDs that have a series configuration. See the Backlight Interface section for more details.

Note

Different displays utilise various pin naming conventions. Be sure to check with your display manufacturer for the correct name and function.

Write Cycle Sequence and Signal Timing

In a write cycle, the PIXXI sends a command or data to the display module through the data bus. The following diagram and table show the write cycle and timing values for the MCU 16-bit interface.



MCU 16-bit Write Cycle Sequence and Signal Timing Diagram

MCU 16-bit Write Signal Timing Values

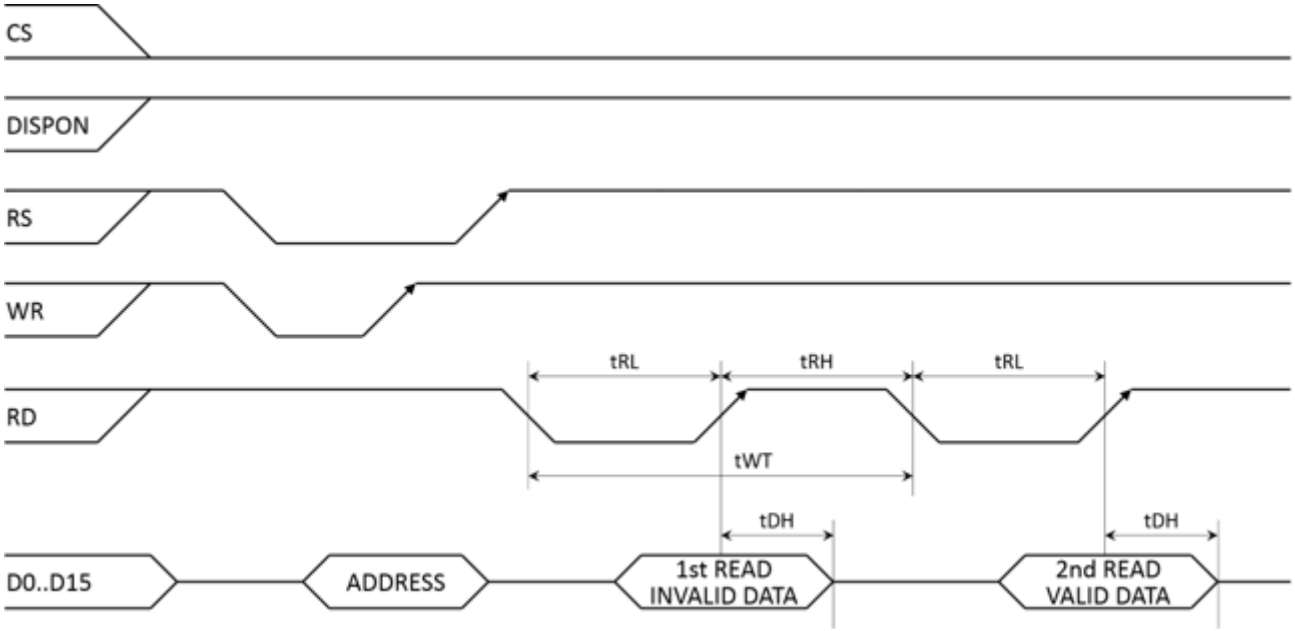
Item	Symbol	Min	Typ	Max	Unit
Write Low Pulse	tWL	50	-	-	ns
Write High Pulse	tWH	50	-	-	ns
Write Bus Cycle Total	tWT	100	-	-	ns
Write Data Setup	tDS	25	-	-	ns

In a write cycle sequence, the DISP-WR signal is driven from HIGH to LOW and then pulled back to HIGH. The display module captures the information from the data bus on the rising edge of DISP-WR. During this time, if the DISP-RS signal is driven to a low level, the display interprets the data on the display bus as command/register address information. If the DISP-RS signal is pulled up high, the display interprets the data as command/register parameter information or as GRAM pixel data.

The process described above is fully automated and the designer need not have to worry about the working mechanics. This is one of the plug-and-play features of the chip. The designer just needs to make the right signal connections.

Read Cycle Sequence and Signal Timing

In a read cycle, the PIXXI reads a command or data from the display module through the data bus. The following diagram and table show the read cycle and timing values for the MCU 16-bit interface.



MCU 16-bit Read Cycle Sequence and Signal Timing Diagram

MCU 16-bit Read Signal Timing Values

Item	Symbol	Min	Typ	Max	Unit
Read Low Pulse	tRL	150	-	-	ns
Read High Pulse	tRH	150	-	-	ns
Read Bus Cycle Total	tRT	300	-	-	ns
Read Data Hold	tDH	75	-	-	ns

The read cycle is a 2-phase process.

Phase 1: Before the desired display data is read, PIXXI must first select the register or the GRAM address location. It does this by performing a write cycle operation of the location.

Phase 2: PIXXI then asserts the DISP-RD signal by driving it from HIGH to LOW and then pulling it back to HIGH during the read cycle. The display module provides the information to the bus during the read cycle on the rising edge of DISP-RD signal.

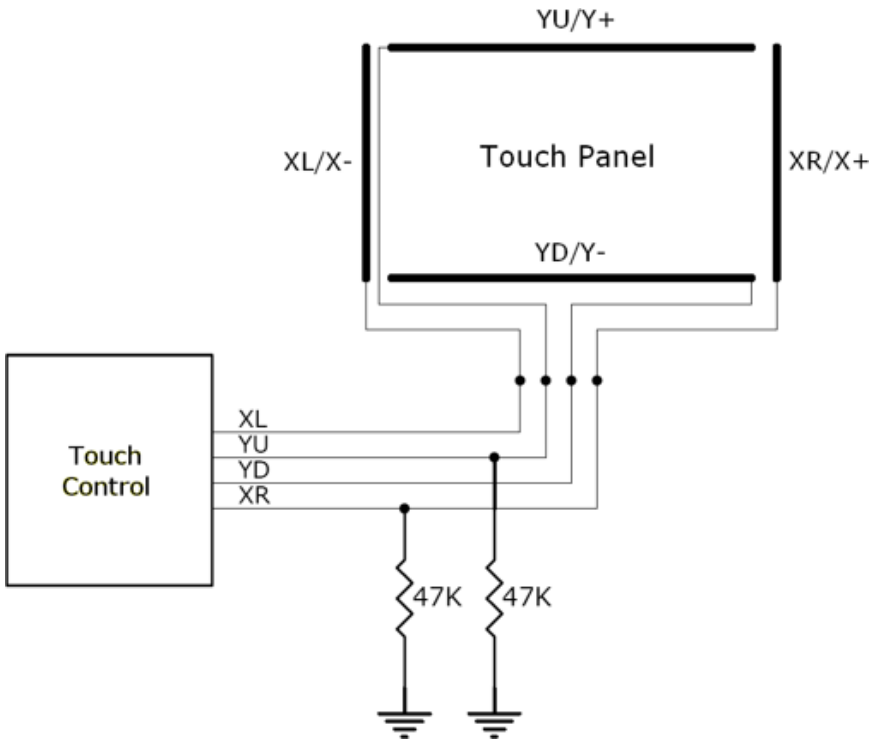
The process described above is fully automated and the designer need not have to worry about the working mechanics. This is one of the plug-and-play features of the chip. The designer just needs to make the right signal connections.

7.2.2. Touch Panel Interface

The PIXXI-44 is configurable to support 4-wire resistive touch panels or capacitive touch panels with a touch controller through I2C interface. For 4-wire resistive touch panels, the internal touch panel controller is only able to directly control touch panels up to 3.5" size. Any touch panels larger than this needs to be used with an external touch controller chip such as the 4DL-763.

Resistive Touch Configuration

The diagram below shows a simplified interface between the PIXXI-44 and a resistive touch panel.



Resistive Touch Interface Connection

Resistive Touch Interface Pins

XR pin (Touch Panel X-Read input):

4-Wire Resistive Touch Screen X-Read analog signal. Connect this pin to XR or X+ signal of the touch panel.

XL pin (Touch Panel X-Drive output):

4-Wire Resistive Touch Screen X Drive signal. Connect this pin to XL or X- signal of the touch panel.

YU pin (Touch Panel Y-Read input):

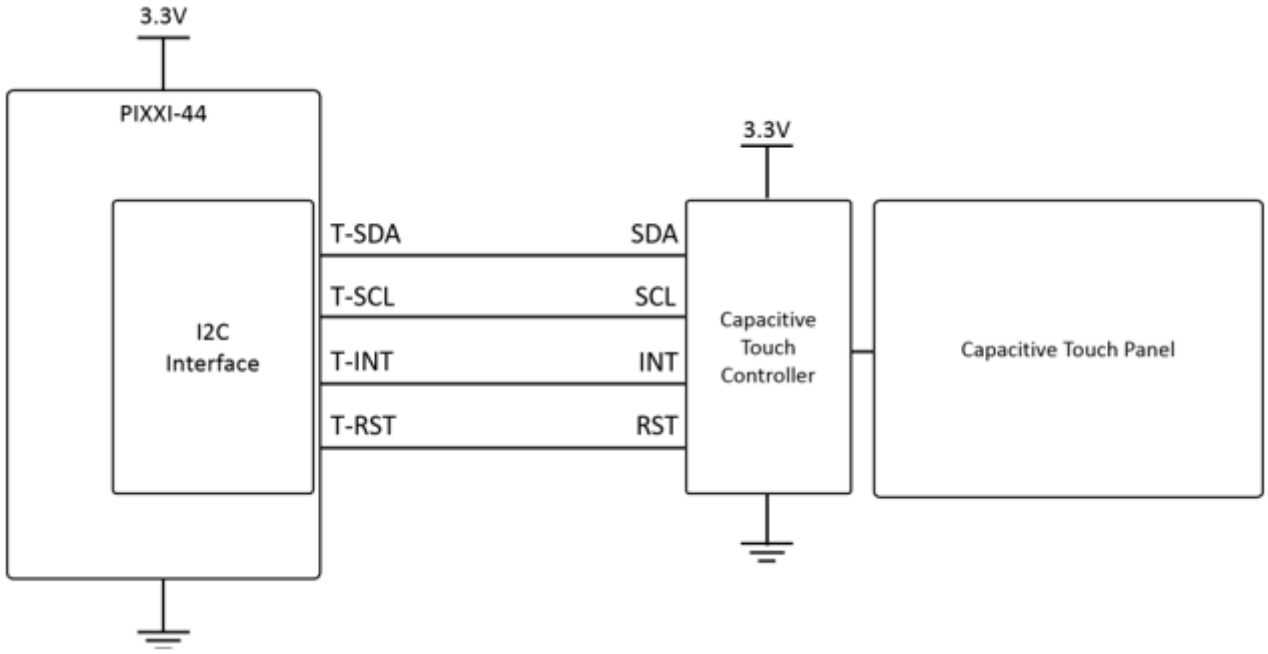
4-Wire Resistive Touch Screen Y-Read analog signal. Connect this pin to YU or Y+ signal of the touch panel.

YD pin (Touch Panel Y-Drive output):

4-Wire Resistive Touch Screen Y Drive signal. Connect this pin to YD or Y- signal of the touch panel.

Capacitive Touch Configuration

The diagram below shows a simplified interface between the PIXXI-44 and a capacitive touch panel.



Capacitive Touch Interface Connection

Capacitive Touch Interface Pins

T-SCL pin (I2C Clock Output):

Connect this pin to the I2C clock input (SCL) signal of the capacitive touch controller.

T-SDA pin (I2C Data In/Out):

Connect this pin to the I2C data in/out signal (SDA) of the capacitive touch controller.

T-INT pin (Touch Interrupt):

Connect this pin to the interrupt signal pin of the capacitive touch controller.

T-RST pin (Touch Reset):

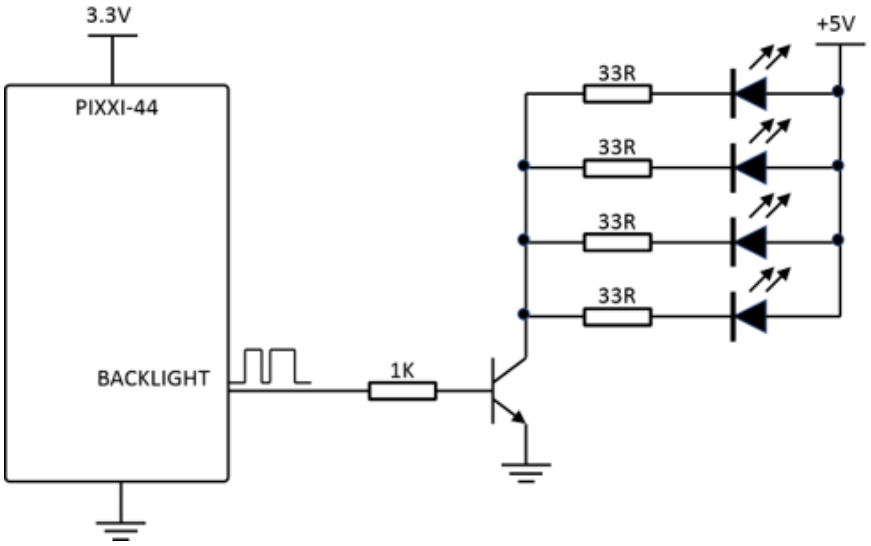
Connect this pin to the reset signal of the capacitive touch controller.

Note

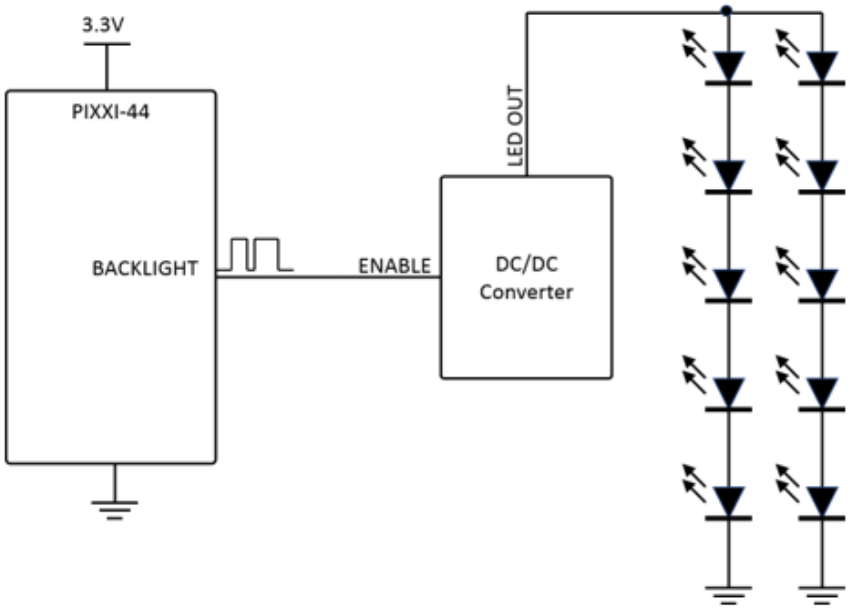
As mentioned in previous sections, there is no need for a low-level access to the touch functionality-related hardware registers when interfacing the PIXXI processor to a touch panel. All access is via high-level 4DG functions. For more information regarding 4DGL functions, please refer to the PIXXI Internal Functions Reference Manual.

7.2.3. Backlight Interface

The backlight control pin is a Pulse Width Modulated (PWM) signal. It can be used with a simple transistor circuit to control backlight LEDs that are in a parallel configuration or it can be used with a more complicated DC/DC high voltage circuits for LEDs that have a series configuration. The diagrams below outline these typical circuit configurations.



Typical Parallel Backlight LEDs Configuration



Typical Series Backlight LEDs Configuration

Note

Backlight control is done with the use of a high level 4DGL function. No low-level access is necessary. For more information regarding 4DGL functions, please refer to the PIXXI Internal Functions Reference Manual.

7.2.4. GPIO Interface

Digital Input and Output

The PIXXI-44 has 19 general purpose input/output (GPIO) pins. The availability of each pin depends on the mode of configuration of the processor. These pins can be accessed individually using bit-wise operations. The table below shows the availability of the pins for digital input and output operations under each mode of configuration. For more information on the different modes of configuration of the processor, refer to the section Device Configuration Modes.

Availability of GPIO Pins in Each Mode of Configuration

GPIO Pin	Pin No.	1N 2N	1R 2R	1C 2C	3N	3R	3C	4N	4R	4C
IO1	25	Yes	Yes	Yes	Yes	Yes	Yes			
IO2	27	Yes	Yes	Yes	Yes	Yes	Yes			
IO3	23	Yes	Yes	Yes	Yes	Yes	Yes			
IO4	24	Yes	Yes	Yes	Yes	Yes	Yes			
IO5	33	Yes	Yes	Yes	Yes	Yes	Yes			
IO6	37	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IO7	38	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IO8	19	Yes			Yes			Yes		
IO9	20	Yes			Yes			Yes		
IO10	41	Yes			Yes					
IO11	42	Yes			Yes					
IO12	1	Yes	Yes	Yes						
IO13	8	Yes	Yes	Yes						
IO14	9	Yes	Yes	Yes						
IO15	10	Yes	Yes	Yes						
IO16	11	Yes	Yes	Yes						
IO17	12	Yes	Yes	Yes				Yes		
IO18	44	Yes	Yes	Yes						
IO19	13							Yes		

On the previous table, pins IO6 and IO7 are available across all modes of configuration. The rest of the pins are available only under a certain mode of configuration of the processor. When choosing a processor mode of configuration, note that unavailable pins are not accessible as they are being used by the processor for other system tasks. Moreover, some pins are configurable for alternative functions such as ADC, UART, I^2, and audio. For more information, refer to the subsequent sections for these peripherals.

Each digital GPIO pin can be individually set as an input or output. Power-up reset default mode for all pins is all inputs. When set as digital inputs, most of the pins are 5.0V-tolerant. However, some pins are 3.3V-tolerant only.

Digital GPIO pins can source/sink 15 mA. For more information, see the sections Pin Configuration Summary and Specifications and Ratings. The table below shows the different configurations available for each pin.

Possible Configurations of GPIO Pins

GPIO Pin	Pin No.	Digital Input	Digital Output
IO1	25	Yes	Yes
IO2	27	Yes	Yes
IO3	23	Yes	Yes
IO4	24	Yes	Yes
IO5	33	Yes	Yes
IO6	37	Yes	Yes
IO7	38	Yes	Yes
IO8	19	Yes	Yes
IO9	20	Yes	Yes
IO10	41	Yes	Yes
IO11	42	Yes	Yes
IO12	1	Yes	Yes
IO13	8	Yes	Yes
IO14	9	Yes	Yes
IO15	10	Yes	Yes
IO16	11	Yes	Yes
IO17	12	Yes	Yes
IO18	44	Yes	Yes
IO19	13	Yes	Yes

Analog Input

GPIO pins IO1, IO2, IO3, and IO4 can serve as analog input pins besides being configurable as digital input or output pins. Power-up reset default mode for all pins is all inputs. For more information on how to use these pins as digital input or output pins, refer to section Digital Input and Output.

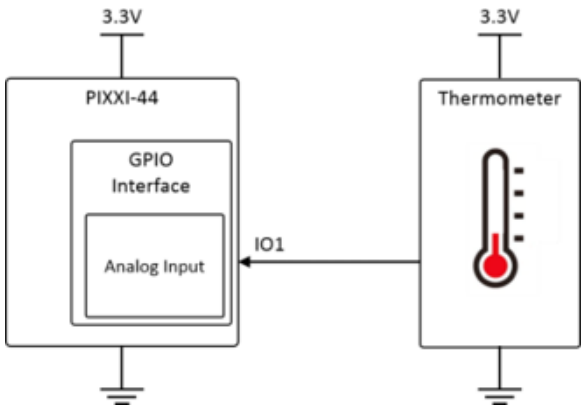
When set as analog inputs, the pins have a 0 to 3.3V range and have 12-bit resolution. The table below shows which pins can be configured as analog inputs and the processor modes of configuration under which these analog inputs are available.

When choosing a processor mode of configuration, note that unavailable pins are not accessible as they are being used by the processor for other system tasks. For more information on the different modes of configuration of the processor, refer to the section Device Configuration Modes.

Availability of Analog Input Pins

GPIO Pin	Pin No.	Mode-1 & Mode-2	Mode-3	Mode-4
IO1	25	Yes	Yes	
IO2	27	Yes	Yes	
IO3	23	Yes	Yes	
IO4	24	Yes	Yes	
IO5	33			
IO6	37			
IO7	38			
IO8	19			
IO9	20			
IO10	41			
IO11	42			
IO12	1			
IO13	8			
IO14	9			
IO15	10			
IO16	11			
IO17	12			
IO18	44			
IO19	13			

The analog inputs can be immediately read at 15000 values per second with 12-bit output. The image below shows an analog input being configured on GPIO IO1 and is used to read an analog temperature from a temperature sensor.

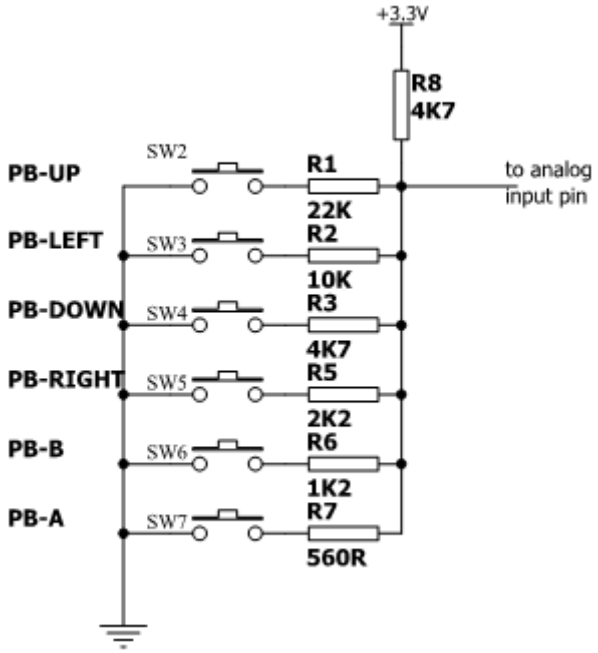


Typical Analog Input Interface Connection Diagram

Note

The example above is an illustration of an analog input connection to the PIXXI-44 processor. It is not the complete circuit, nor does it illustrate best practice.

A network of button and resistors (which act as voltage dividers) can also be connected to any of the analog input pins. The A/D converter of the analog pin would then internally read the analogue value and decode it accordingly. The decoded value could then be used in a 4DGL program for any purpose. This allows the analog input pin to be used to interpret the status of a multi-state switch. The diagram below shows how multiple buttons and resistors can be connected and interfaced to an analog input pin.



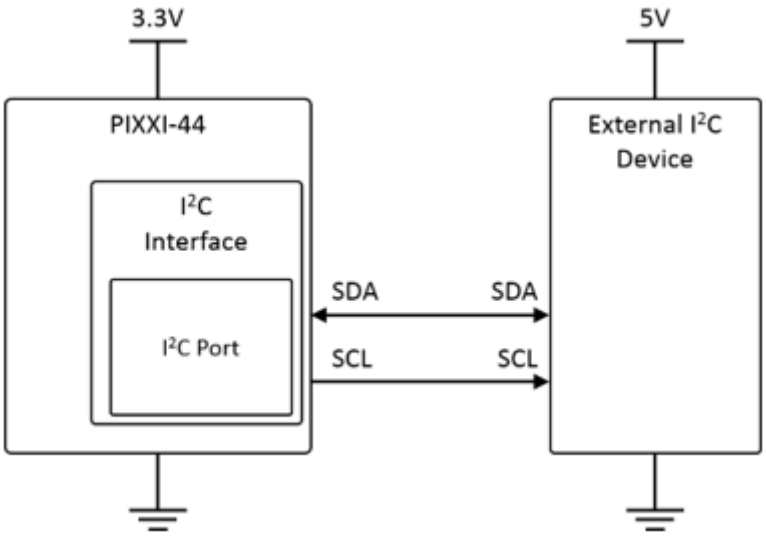
Connection Diagram for Multiple Buttons and Resistors

Note

Due to the unique architecture of the device, there is no need for a low-level access to the digital input and output, and analog-to-digital converter hardware registers when using the PIXXI-44 processor. All access is via high-level 4DGL functions. For more information regarding 4DGL functions, please refer to the PIXXI Internal Functions Reference Manual.

7.2.4.1. I2C Interface

The I2C peripheral supports standard, full speed, and fast modes. The PIXXI-44 can function as a master only in an I^2 bus. The figure below shows a typical connection between the I^2 interface of the PIXXI-44 to that of an external device.



Typical I2C Interface Connection

Note

This example is an illustration of I2C connection to the PIXXI-44 processor. It is not the complete circuit nor illustrates best practice.

The PIXXI-44 processor has three I^2C channels - I^2C1, I^2C2, and I^2C3. The availability of each channel depends on the selected mode of configuration of the processor. Moreover, the I^2C SDA and SCL pins are allocated on fixed pins. These pins can be used for I^2C communication, provided that the desired I^2C channel to be used is available under the selected processor mode of configuration.

I2C Interface Pins

SCL1 (I2C Clock Output):

I2C clock output pin, SCL1. Connect this pin to the SCL pin of an external I2C device.

SDA1 (I2C Data In/Out):

I2C data input/output pin, SDA1. Connect this pin to the SDA pin of an external I2C device.

SCL2 (I2C Clock Output):

I2C clock output pin, SCL2. Connect this pin to the SCL pin of an external I2C device.

SDA2 (I2C Data In/Out):

I2C data input/output pin, SDA2. Connect this pin to the SDA pin of an external I2C device.

SCL3 (I2C Clock Output):

I2C clock output pin, SCL3. Connect this pin to the SCL pin of an external I2C device.

SDA3 (I2C Data In/Out):

I2C data input/output pin, SDA3. Connect this pin to the SDA pin of an external I2C device.

The table below shows which GPIO pins are configurable as I2C SDA and SCL pins and the processor modes of configurations under which these pins are available. When choosing a processor mode of configuration, note that unavailable pins are not accessible as they are being used by the processor for other system tasks. For more information on the different modes of configuration of the processor, refer to the section Device Configuration Modes.

Availability of I2C Pins

GPIO Pin	Pin No.	Mode-1 & Mode-2 N	Mode-1 & Mode-2 R	Mode-1 & Mode-2 C	Mode-3 N	Mode-3 R	Mode-3 C	Mode-4 N	Mod
IO1	25	SCL2	SCL2	SCL2	SCL2	SCL2	SCL2		
IO2	27	SDA2	SDA2	SDA2	SDA2	SDA2	SDA2		
IO6	37	SDA1	SDA1	SDA1	SDA1	SDA1	SDA1	SDA1	SDA
IO7	38	SCL1	SCL1	SCL1	SCL1	SCL1	SCL1	SCL1	SCL
IO8	19	SCL3			SCL3			SDA3	
IO11	42	SDA3			SDA3				
IO17	12							SCL3	

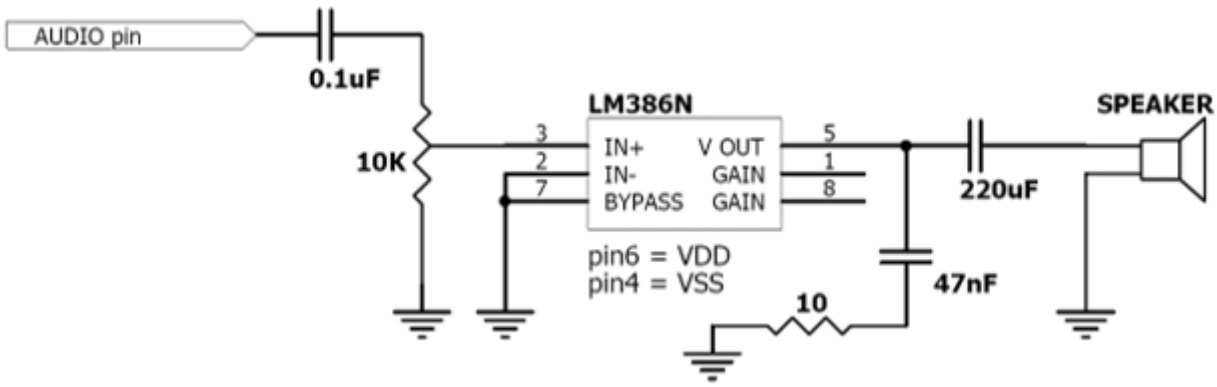
Note

Due to the unique architecture of the device, there is no low-level access to the I2C hardware, and all access is via high-level 4DGL functions. For more information regarding 4DGL functions, please refer to the PIXXI Internal Functions Reference Manual.

7.2.4.2. Audio Interface

The audio support in the PIXXI-44 processor makes it better than its peers in the graphics processor range. A simple instruction empowers the user to execute the audio files. Audio operation can be carried out simultaneously with the execution of other necessary instructions. The PIXXI-44 provides a 16-bit DAC/PWM audio output to be used with an external audio amplifier. PWM ensures better sound quality with a volume range of 8 to 127.

The circuit in the figure below shows a low-cost implementation.



Typical Audio Interface Connection

The table below shows which pins are utilized by the processor as audio pins under each mode of configuration of the processor. As can be seen in the table, audio support is available only under Mode-1, Mode-2, and Mode-3. When choosing a processor mode of configuration, note that unavailable pins are not accessible as they are being used by the processor for other system tasks. For more information on the different modes of configuration of the processor, refer to the section Device Configuration Modes.

Availability of Audio Pins

Pin No.	Mode-1 & Mode-2	Mode-3	Mode-:4
12		**Yes (AUDIOENB)**	
14	**Yes (AUDIOENB)**		
43	**Yes (AUDIO)**	**Yes (AUDIO)**	

Audio Interface Pins

AUDIO (Audio PWM output):

External Amplifier Output pin. This pin provides a 16-bit DAC/PWM audio output to use with an external audio amplifier. If unused, then this pin must be left open or floating.

AUDENB (Audio Enable output):

External Amplifier enable pin. This pin provides ON/OFF amplifier control. If unused, then this pin must be left open or floating. [**LOW:** Disable external Audio amplifier, **HIGH:** Enable external Audio amplifier]

Note

Due to the unique architecture of the device, there is no low-level access to the audio peripheral and all access is via high-level 4DGL functions. For more information regarding 4DGL functions, please refer to the PIXXI Internal Functions Reference Manual.

7.2.4.3. Configurable UART Interface

The PIXXI-44 processor has two hardware asynchronous serial ports, referred to as COM0 and COM1. COM0 is a fixed, dedicated port while COM1 is a configurable port. These ports can communicate with external serial devices. For more information regarding primary features, single byte timing, and typical interface connection of the UART peripheral, refer to the UART Interface section under the Fixed Hardware Layer section.

The table below shows which GPIO pins are configurable as TX1 and RX1 pins and the processor modes of configurations under which these pins are available. When choosing a processor mode of configuration, note that unavailable pins are not accessible as they are being used by the processor for other system tasks. For more information on the different modes of configuration of the processor, refer to the section Device Configuration Modes.

Availability of Configurable UART Pins

GPIO Pin	Pin No.	Mode-1 & Mode-2	Mode-3	Mode-4
IO4	24	**Yes (TX1)**	**Yes (TX1)**	
IO5	33	**Yes (RX1)**	**Yes (RX1)**	

Configurable UART Interface Pins

TX1 pin (Serial Transmit COM1):

Asynchronous Serial port COM1 transmit pin, TX1. Connect this pin to external serial device receive (Rx) signal.

RX1 pin (Serial Receive COM1):

Asynchronous Serial port COM1 receive pin, RX1. Connect this pin to external serial device transmit (Tx) signal. This pin is 5.0V tolerant.

Note

Due to the unique architecture of the device, there is no low-level access to the UART peripheral, and all access is via high-level 4DGL Functions. For more information regarding 4DGL functions, please refer to the PIXXI Internal Functions Reference Manual.

7.2.5. Fixed Hardware Layer

This section describes in detail the fixed hardware interface.

7.2.5.1. System Power and Clock

System Power and Clock Pins

VCC pins (Device Supply Voltage):

Device supply voltage pins. These pins must be connected to a regulated supply voltage in the range of 3.0 Volts to 3.6 Volts DC. Nominal operating voltage is 3.3 Volts.

GND pins (Device Ground):

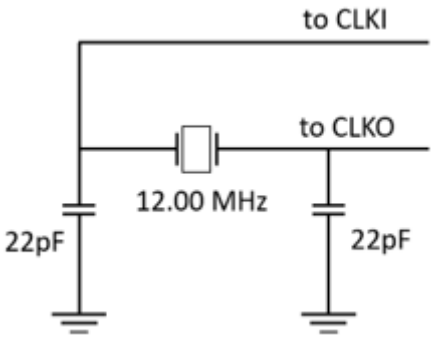
Device ground pins. These pins must be connected to system ground.

RESET pin (Device Master Reset):

Device Master Reset pin. An active low pulse of greater than 2 micro-seconds will reset the device. Connect a resistor (1K through to 10K, nominal 4.7K) from this pin to VCC. Only use open collector type circuits to reset the device if an external reset is required. This pin is not driven low by any internal conditions.

CLKI, CLKO pins (Device Oscillator Inputs):

CLKI and CLKO are the device oscillator pins. Connect a 12MHz AT strip cut crystal with 22pF capacitors from each pin to GND as shown in the diagram below.

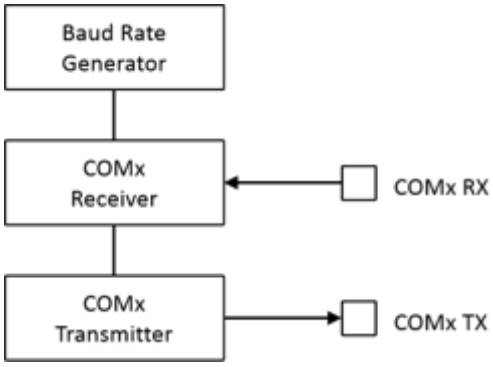


Crystal Oscillator Connection

7.2.6. UART Interface

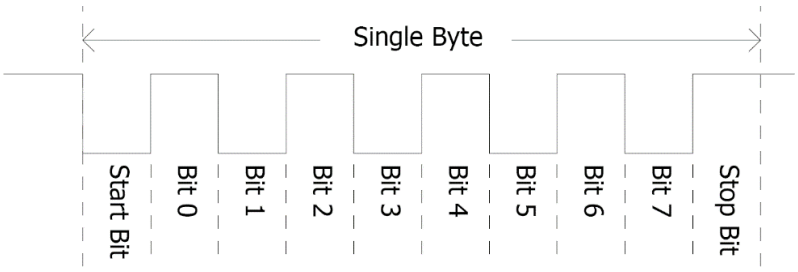
The PIXXI-44 processor has two hardware asynchronous serial ports, referred to as COM0 and COM1. COM0 is a fixed, dedicated port while COM1 is configurable port. These ports can communicate with external serial devices. The primary features are:

- Full-Duplex 8-bit data transmission and reception.
- Data format: 8 bits, No Parity, 1 Stop bit.
- Independent Baud rates from 300 baud up to 2187500 baud.
- Single byte transmits and receives or a fully buffered service. The buffered service feature runs in the background capturing and buffering serial data without the user application having to constantly poll any of the serial ports. This frees up the application to service other tasks.



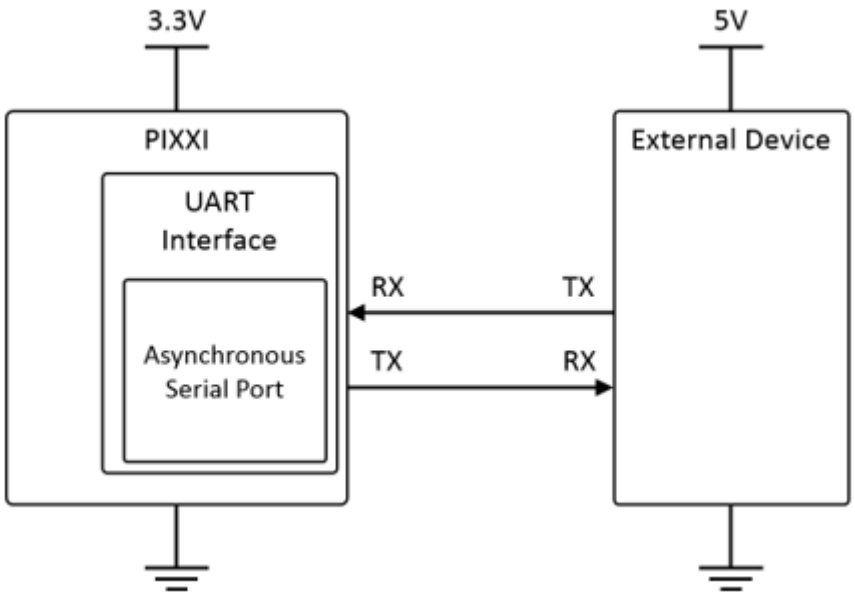
Block Diagram of the UART Interface

A single byte serial transmission consists of the start bit, 8-bits of data followed by the stop bit. The start bit is always 0, while a stop bit is always 1. The LSB (Least Significant Bit, Bit 0) is sent out first following the start bit. The figure below shows a single byte transmission timing diagram.



Timing Diagram of a Single Byte

The figure below shows a typical connection between the UART interface of the PIXXI-44 to that of an external 5-volt device. The RX pin of the PIXXI-44 is 5-volt-tolerant. The external 5-volt device should be able to interpret the 3.3-volt logic of the TX pin of the PIXXI-44.



Typical UART Interface Connection

Fixed UART Interface Pins

TX0 pin (Serial Transmit COM0):

Asynchronous Serial port COM0 transmit pin, TX0. Connect this pin to external serial device receive (Rx) signal. This pin is 5.0V tolerant.

RX0 pin (Serial Receive COM0):

Asynchronous Serial port COM0 receive pin, RX0. Connect this pin to external serial device transmit (Tx) signal. This pin is 5.0V tolerant.

Programming Interface

The dedicated serial port of the processor is also the primary interface for 4DGL user program downloads and chip configuration PmmC programming. Once the compiled 4DGL application program (EVE bytecode) is downloaded and the user code starts executing, the serial port is then available to the user application. Refer to the In Circuit Serial Programming section for more details on PmmC/Firmware programming.

Note

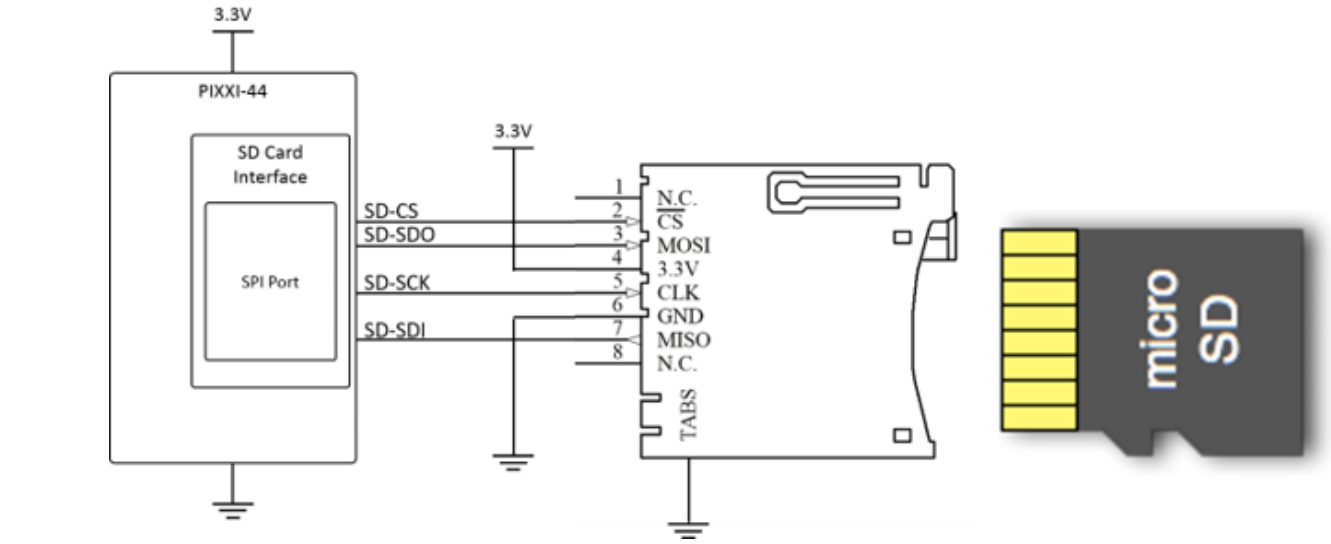
Due to the unique architecture of the device, there is no low-level access to the UART peripheral, and all access is via high-level 4DGL Functions. For more information regarding 4DGL functions, please refer to the **PIXXI Internal Functions Reference Manual.**

7.2.6.1. SD Card Interface

The PIXXI-44 processor supports SD, micro-SD and MMC memory cards via its dedicated hardware SPI interface. The memory card is used for all multimedia file retrieval such as images, animations and movie clips, and the SPI interface is dedicated for this purpose only. The memory card can also be used as general-purpose storage for data logging applications (RAW and FAT16 format support). Support is available for micro-SD with up to 2GB capacity and for high capacity HC memory cards starting from 4GB and above.

The dedicated SPI port is clocked at 35MHz. It is highly advised to keep the SD connector close to the PIXXI and all PCB traces short as possible.

The diagram below illustrates a typical connection between the PIXXI and a serial flash memory chip.



Typical SD Card Interface

SD Card Interface Pins

SD-SDI pin (SPI Serial Data Input):

The SD Card SPI Serial Data Input (SD-SDI) signal. SD memory card use only. Connect this pin to the SPI Serial Data Out (SDO) signal of the memory card.

SD-SDO pin (SPI Serial Data Out):

The SD Card SPI Serial Data Output (SD-SDO) signal. SD memory card use only. Connect this pin to the SPI Serial Data In (SDI) signal of the memory card.

SD-SCK pin (SPI Serial Clock Out):

SD Card SPI Serial Clock output (SD-SCK) signal. SD memory card use only. Connect this pin to the SPI Serial Clock (SCK) signal of the memory card.

SD-CS pin (Chip Select):

SD Card Chip Select (SD-CS) signal. SD memory card use only. Connect this pin to the Chip Enable (CS) signal of the memory card.

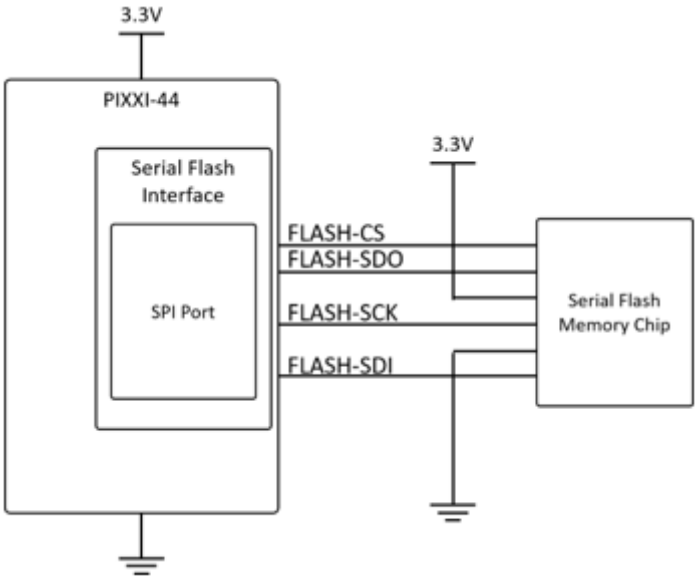
Note

As mentioned in previous sections, there is no need for a low-level access to the SPI hardware registers when interfacing the PIXXI processor to a SD card. All access is via high-level 4DGL functions. For more information regarding 4DGL functions, please refer to the PIXXI Internal Functions Reference Manual.

7.2.6.2. Serial Flash Memory Interface

The PIXXI-44 processor supports serial flash memory chips via its dedicated hardware SPI interface. The serial flash memory chip is used for all multimedia file retrieval such as images, animations and movie clips, and the SPI interface is dedicated for this purpose only. Support is available for serial flash memory chip with up to 16 MB capacity.

The dedicated SPI port is clocked at 35MHz. It is highly advised to keep the serial flash memory chip close to the PIXXI and all PCB traces short as possible. The diagram below illustrates a typical connection between the PIXXI and a serial flash memory chip.



Typical Serial Flash Memory Chip Interface

Serial Flash Interface Pins

Serial Flash-SDI pin (SPI Serial Data Input):

The Serial Flash SPI Serial Data Input (FLASH-SDI) signal. Connect this pin to the SPI Serial Data Out (SDO) signal of the Serial Flash memory chip.

Serial Flash-SDO pin (SPI Serial Data Out):

The Serial Flash SPI Serial Data Output (FLASH -SDO) signal. Connect this pin to the SPI Serial Data In (SDI) signal of the Serial Flash memory chip.

Serial Flash-SCK pin (SPI Serial Clock Out):

The Serial Flash SPI Serial Clock output (FLASH -SCK) signal. Connect this pin to the SPI Serial Clock (SCK) signal of the Serial Flash memory chip.

Serial Flash-CS pin (SPI Serial Chip Select):

Serial Flash Chip Select (FLASH -CS) signal. Serial Flash memory chip use only. Connect this pin to the Chip Enable (CS) signal of the Flash memory chip

Note

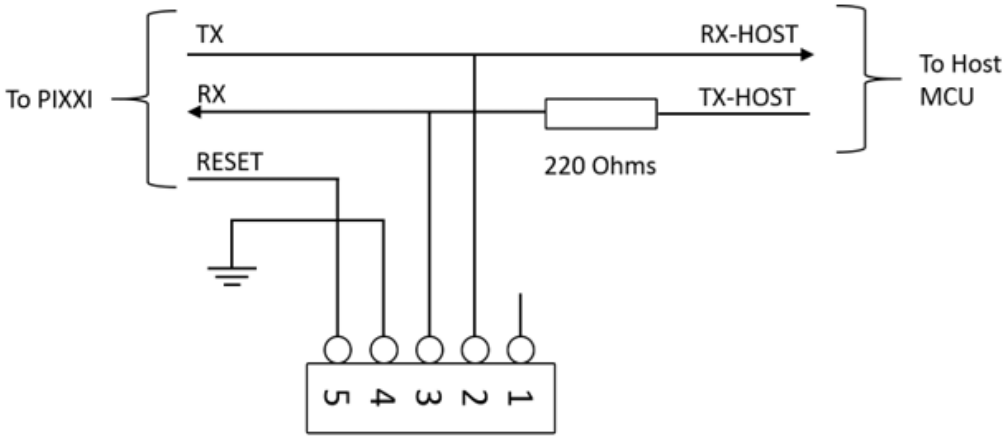
As mentioned in previous sections, there is no need for a low-level access to the SPI hardware registers when interfacing the PIXXI processor to a serial flash memory device. All access is via high-level 4DGL functions. For more information regarding 4DGL functions, please refer to the PIXXI Internal Functions Reference Manual.

8. In-Circuit Serial Programming

The PIXXI processor is a custom graphics processor. All functionality including the high-level commands are built into the chip. This chip level configuration is available as a Firmware/PmmC (Personality-module-micro-Code) file.

A PmmC file contains all of the low-level micro-code information (analogy of that of a soft silicon) which define the characteristics and functionality of the device. The ability of programming the device with a PmmC file provides an extremely flexible method of customising as well as upgrading it with future enhancements.

A PmmC file can only be programmed into the device via its serial port and an access to this must be provided for on the target application board. This is referred to as In Circuit Serial Programming (ICSP). The figure below provides a typical implementation for the ICSP interface.



Typical ICSP Interface Connection

The PmmC file is programmed into the device with the aid of Workshop4, the 4D Labs IDE software (see the section Workshop4 IDE). To provide a link between the PC and the ICSP interface, a specific 4D programming module is required and is available from 4D Systems.

Using a non-4D programming interface could damage your processor and **void your Warranty**.

> **Note**
>
> The PIXXI processor is shipped blank and must be programmed with the PmmC configuration file.

9. Programming Language

The PIXXI processor belongs to a family of processors powered by a highly optimised soft-core virtual engine, EVE (Extensible Virtual Engine).

EVE is a proprietary, high performance virtual-machine with an extensive byte-code instruction set optimised to execute compiled 4DGL programs. 4DGL (4D Graphics Language) was specifically developed from ground up for the EVE engine core. It is a high-level language which is easy to learn and simple to understand yet powerful enough to tackle many embedded graphics applications.

4DGL is a graphics-oriented language allowing rapid application development, and the syntax structure was designed using elements of popular languages such as C, Basic, Pascal and others.

Programmers familiar with these languages will feel right at home with 4DGL. It includes many familiar instructions such as `IF..ELSE..ENDIF, WHILE..WEND, REPEAT..UNTIL, GOSUB..ENDSUB, GOTO, PRINT` as well as some specialised instructions `SERIN, SEROUT, GFX_LINE, GFX_CIRCLE` and many more.

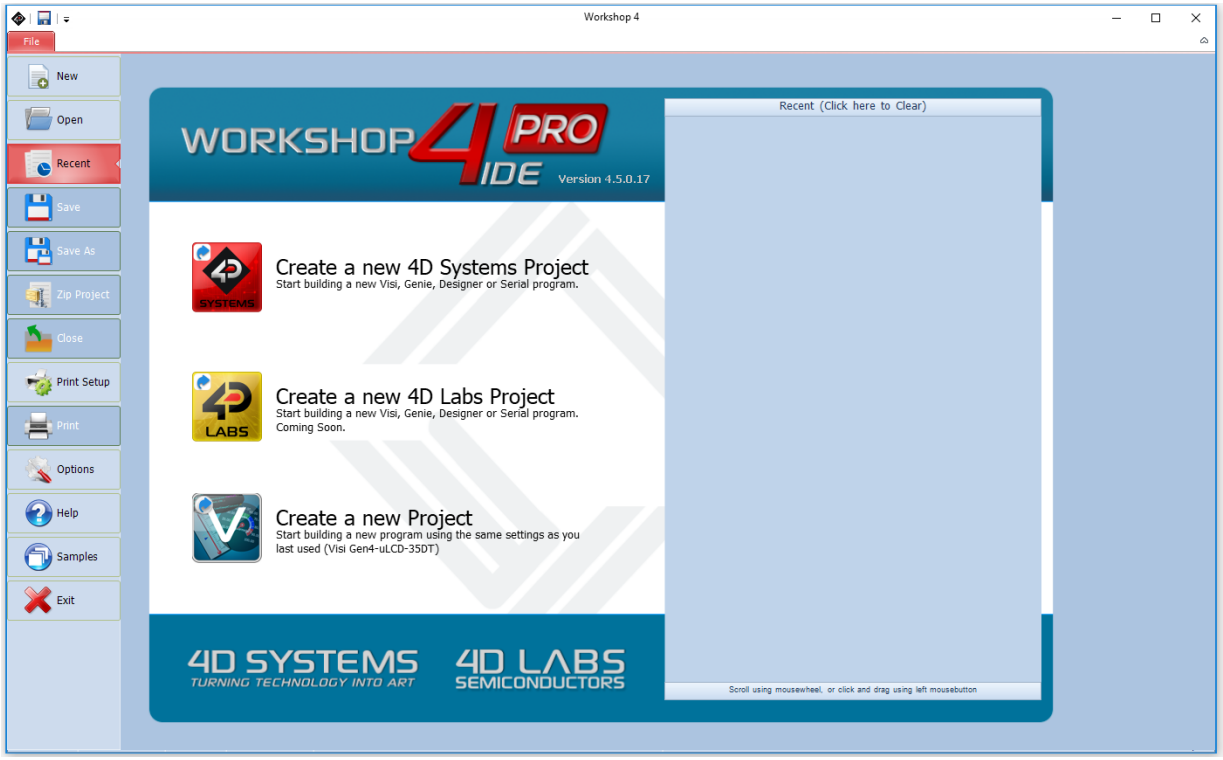
For detailed information pertaining to the 4DGL language, please refer to the following documents:

- 4DGL Programmers Reference Manual
- PIXXI Internal Functions Manual

To assist with the development of 4DGL applications, the Workshop4 IDE combines a full-featured editor, a compiler, a linker and a downloader into a single PC-based application. It's all you need to code, test and run your applications.

10. Workshop4 IDE

Workshop4 is a comprehensive software IDE that provides an integrated software development platform for all of the 4D family of processors and modules. The IDE combines the Editor, Compiler, Linker and Downloader to develop complete 4DGL application code. All user application code is developed within the Workshop4 IDE.



The Workshop4 IDE supports multiple development environments for the user, to cater to different user requirements and skill levels.

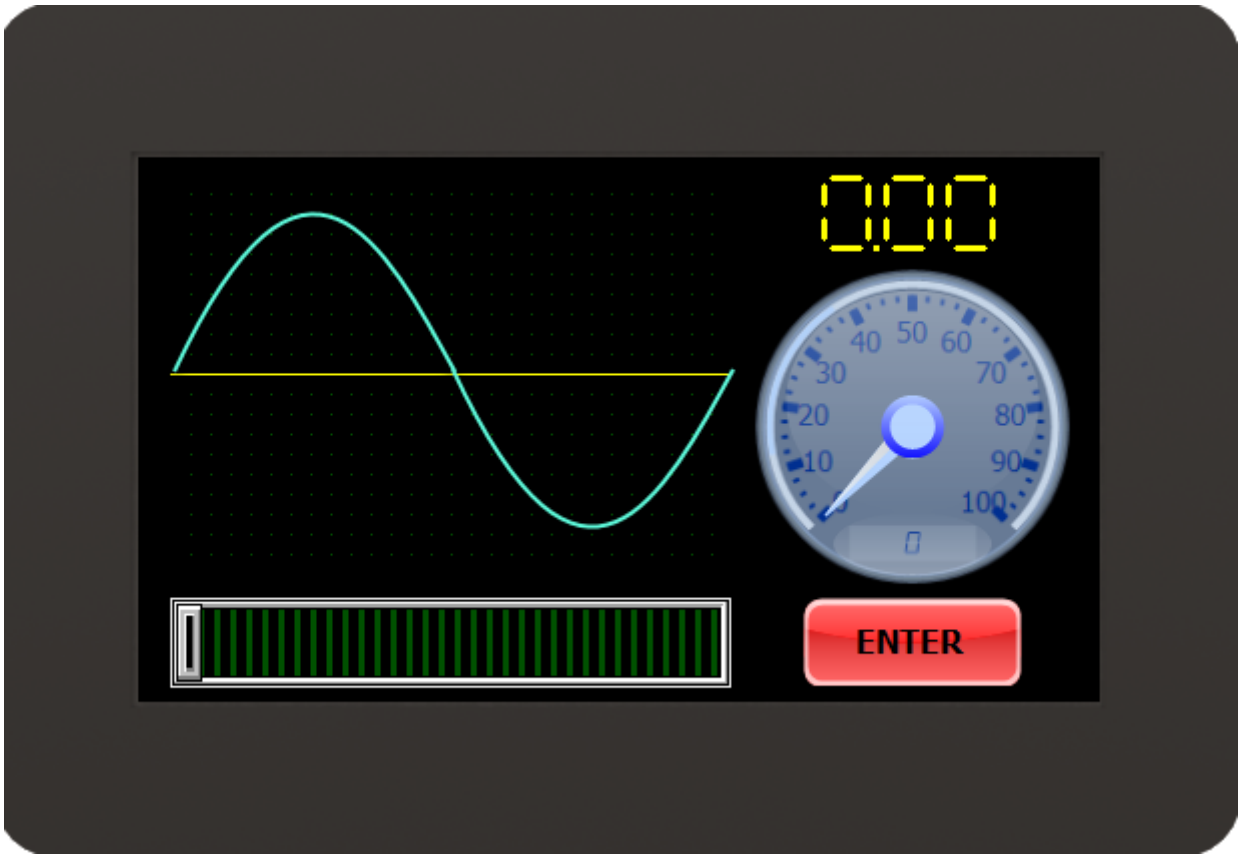
- The **Designer** environment enables the user to write 4DGL code in its natural form to program the range of 4D System's intelligent displays.
- A visual programming experience, suitably called **ViSi**, enables drag-and-drop type placement of objects to assist with 4DGL code generation and allows the user to visualise how the display will look while being developed.
- An advanced environment called **ViSi-Genie** doesn't require any 4DGL coding at all, it is all done automatically for you. Simply lay the display out with the objects you want, set the events to drive them and the code is written for you automatically. This can be extended with additional features when a Workshop4 PRO license is purchased from the 4D Systems website. Extended Advanced features for ViSi-Genie are available in the PRO version of WS4. Further details are explained in the ViSi Genie section of the Workshop4 documentation.
- A **Serial** environment is also provided to transform the display module into a slave serial module, allowing the user to control the display from any host microcontroller or device with a serial port.

For more information regarding these environments, refer to the Workshop4 manuals.

The Workshop4 IDE is available from the 4D Systems website.

11. Widgets

Widgets are essential elements of any graphical user interface design. The Worskhop4 IDE provides a variety of widgets to cater to different user application requirements. Widgets may come in the form of buttons and sliders (for user interaction), LEDs (for status indication), digits, and scope and gauges (for displaying values). Worskhop4 IDE also provides a facility for users to create and manipulate their own custom widgets. The image below shows a typical graphical user interface design containing several widgets.



In the ViSi-Genie environment, adding widgets to a user interface design is as easy as drag-and-dropping the widgets from the widgets selection pane to the WYSIWYG (What-You-See-Is-What-You-Get) area. The properties of the widgets can be configured through the object inspector. ViSi-Genie will automatically handle the operation of the widgets during runtime.

In the ViSi environment, the procedure for adding widgets to a project is similar to that in the ViSi-Genie environment. The user will then have to define the behaviour of the widgets during runtime through 4DGL coding.

In the Designer environment, widgets are rendered on the display and their behaviour is defined through 4DGL coding.

With respect to method of implementation, PIXXI widgets can be classified into three different types:

- **Graphics Composer Image (GCI) Widgets**, Image based widgets generated by Workshop4 that are stored in the microSD Card or External Flash memory.
- **Internal Functions (PmmC) Widgets**, these are widgets that are inside the Pixxi device and accessed via 4DGL internal function calls.
- **Inherent Widgets**, widgets that are generated and rendered in real-time by utilising proprietary algorithms to access graphical information stored in the External Flash memory.

PIXXI processors can use either GCI or Inherent widgets depending on the PmmC loaded. All PmmC widgets are available across all PIXXI PmmCs.

Listed on the table below are the advantages and disadvantages of each widget type.

Widget	Advantages	Disadvantages
GCI Widgets	- High-quality widgets - Display images and video clips - Cost effective when used with external flash memory	- Requires microSD card or external flash memory - Requires large amount of external memory space for rendering widgets
Internal (PmmC) Widgets	- Basic widget types available - Available on all types of PIXXI PmmC - No need for external memory storage	- No images and video clips - Consumes User Internal Flash on Processor
Inherent Widgets	- High-quality widgets	- No images and video clips - Requires external flash memory

The subsequent sections discuss the different widgets available to the user.

For more information, please refer to the Workshop4 Widgets Reference Manual.

11.1. GCI Widgets

The Graphics Composer Image (GCI) Widgets, are Image-based widgets that are generated by the Graphics Composer integrated in the Workshop4 IDE. These widgets are compiled into a GCI graphics file that is stored to the micro-SD or External Flash Memory, accessible to the processor for rendering on the display during runtime. GCI widgets can be classified further into standard and smart widgets. Standard widgets are available in the standard version of Workshop4. These are different from smart widgets, which are available only in the PRO version of Workshop4. For more information, refer to the Workshop4 Widgets Reference Manual.

11.1.1. Standard Widgets

Standard widgets are widgets available in the standard version of Workshop4.

11.1.1.1. Button Widgets

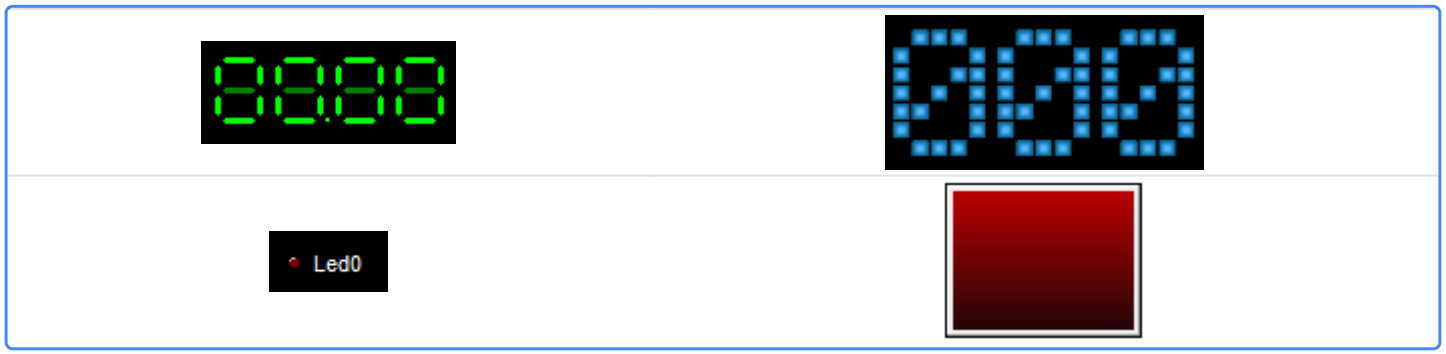
These are widgets commonly used for receiving touch inputs from the user.

Standard Button Widgets

11.1.1.2. Digits Widgets

These are widgets commonly used for displaying values or status information.

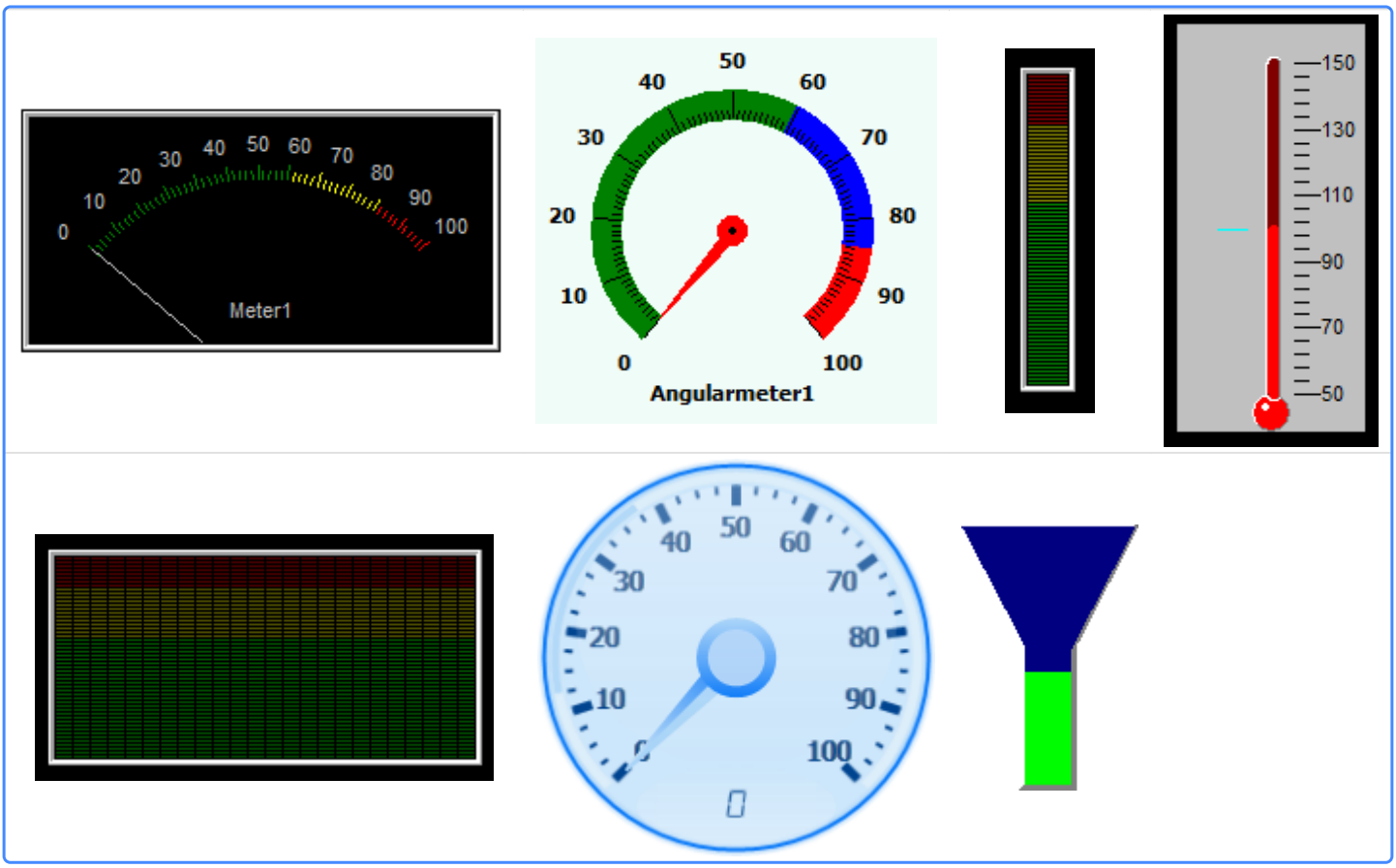
Standard Digits Widgets



11.1.1.3. Gauge Widgets

These are widgets commonly used for displaying values.

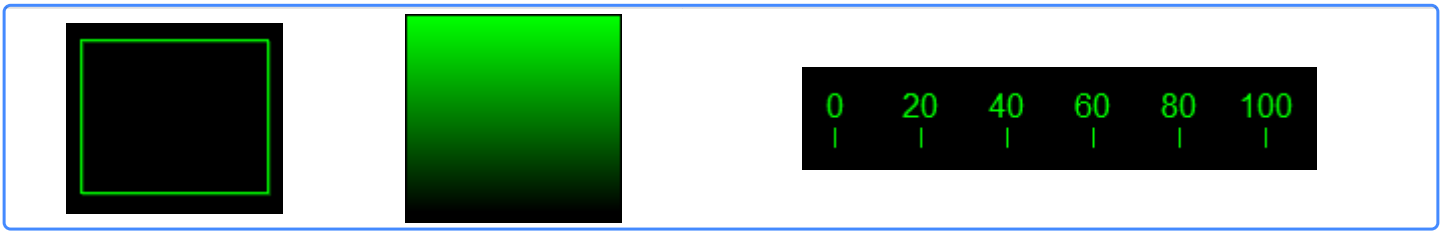
Standard Gauge Widgets



11.1.1.4. Background Widgets

These are widgets commonly used for creating basic background images like border, gradient, and scale.

Standard Background Widgets



11.1.1.5. Label Widgets

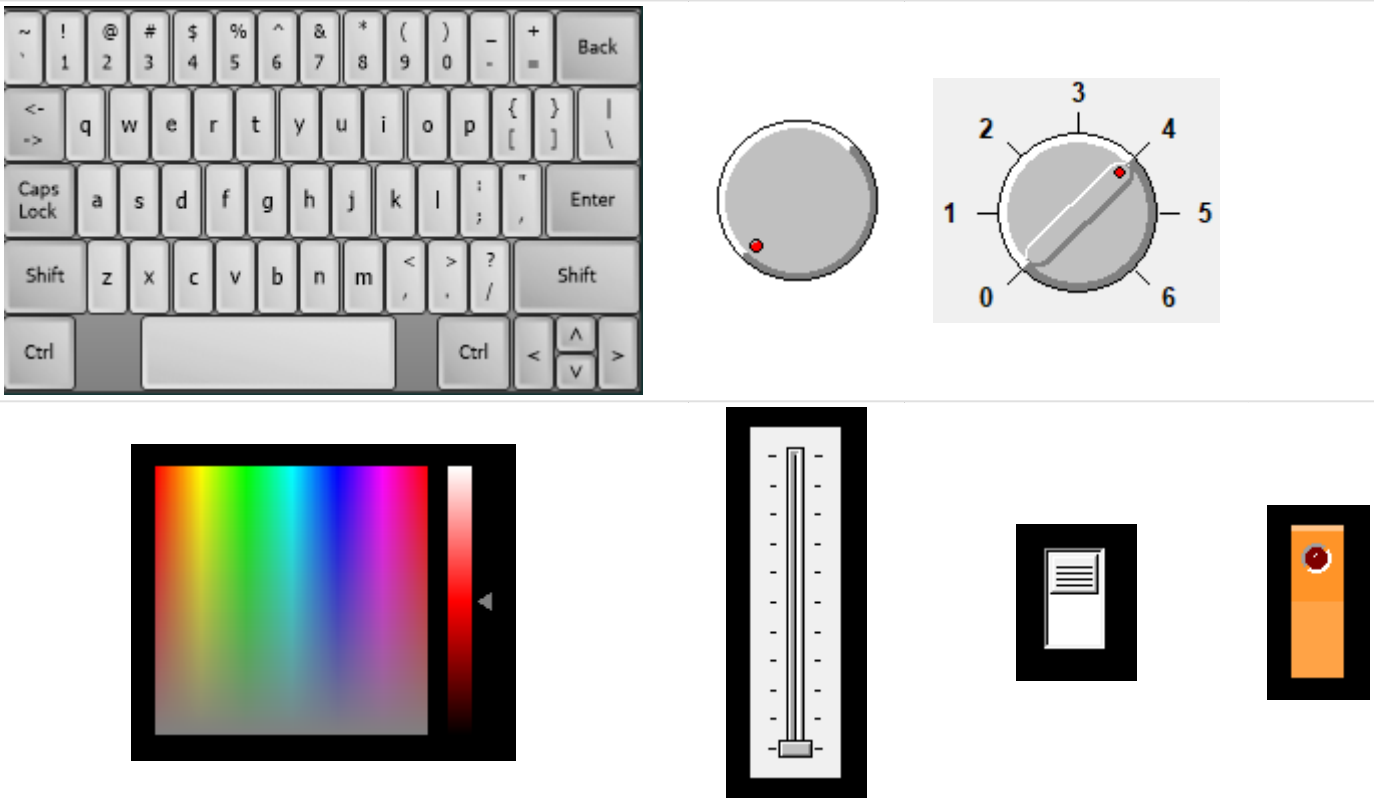
These are widgets commonly used for displaying text information.

Standard Label Widgets

11.1.1.6. Input Widgets

These are widgets commonly used for receiving touch inputs from the user. Below are examples:

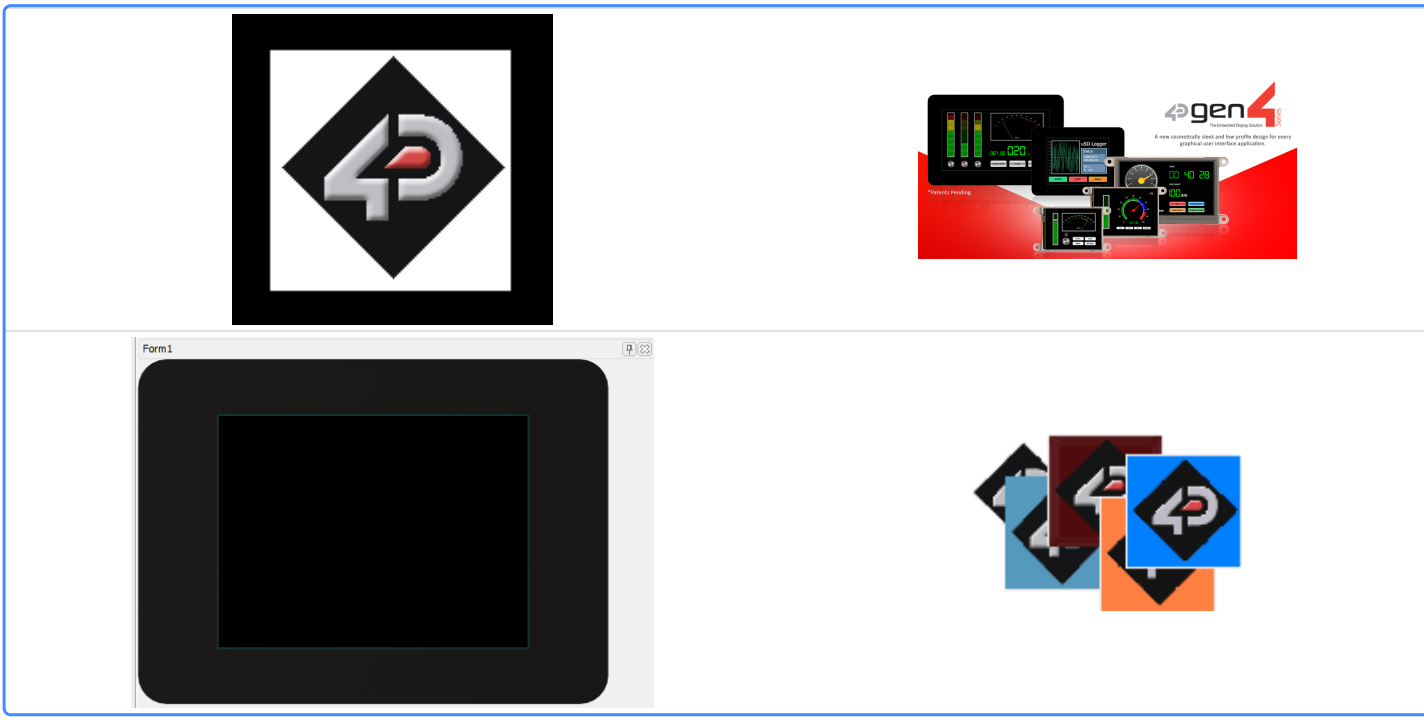
Standard Input Widgets



11.1.1.7. System/Media Widgets

These are widgets commonly used for displaying or handling video, images and media.

Standard System/Media Widgets



11.1.2. Smart Widgets

Smart widgets are available only in the PRO version of Workshop4. Smart widgets are custom widgets generated using the Smart Widgets Editor tool. The Smart Widgets Editor tool is a powerful utility that can be used to create complex widgets with up to six layers, including the layer for the base image. The layers can be arranged in any desired order. Each layer can contain one or more images arranged in sequence that can be manipulated in a variety of ways. Image manipulation options include horizontal motion, vertical motion, and angular motion. Two or more layers can be linked to produce synchronized movements of images. This enables the generation of complex widgets with multiple moving parts. For more information, refer to the Smart Widgets Editor User Guide.

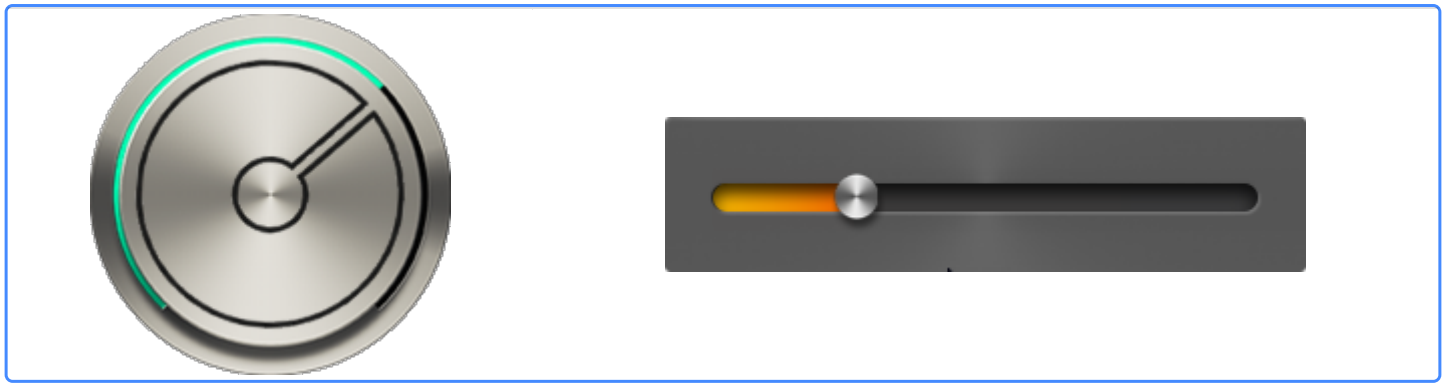
As of writing, there are three types of smart widgets - smart gauge, smart knob, and smart slider. The following subsections show examples of these widgets.

11.1.2.1. Smart Gauge Widget

Smart Gauge Widget

11.1.2.2. Smart Input Widgets

Smart Input Widget



11.2. Internal (PmmC) Widgets

The Internal Functions (PmmC) Widgets are widgets that are generated using 4DGL Internal Functions. These widgets are available in the standard version of Workshop4. For detailed discussion on this type of widgets, refer to the Workshop4 Widgets Reference Manual.

The following subsections show examples of these widgets.

11.2.1. Button Widgets

These are widgets commonly used for receiving touch inputs from the user.

Internal Button Widgets

11.2.2. Digits Widgets

These are widgets commonly used for displaying values or status information.

Internal Digits Widgets

11.2.3. Input Widgets

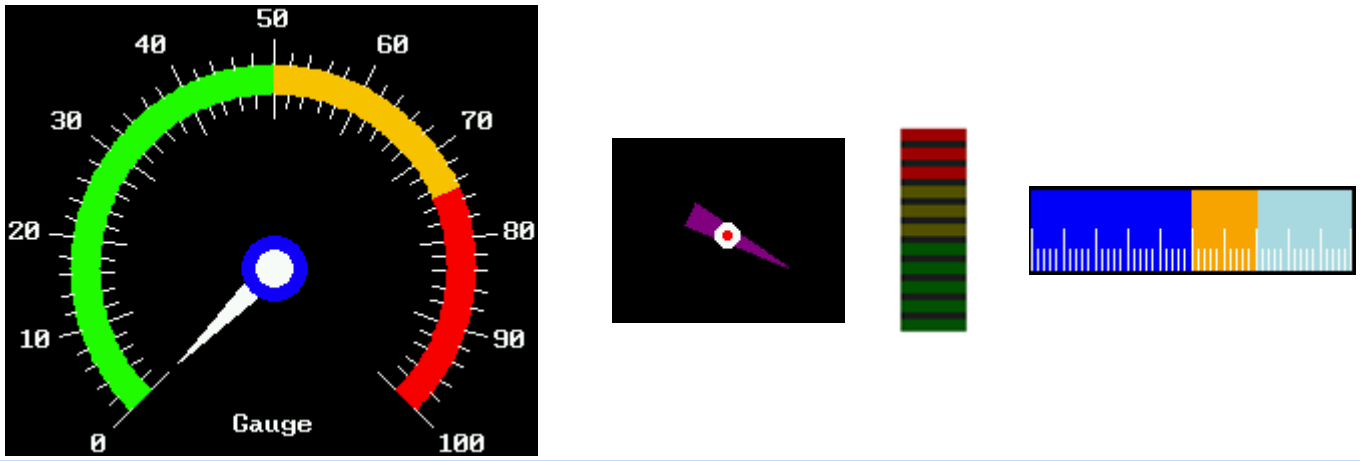
These are widgets commonly used for receiving touch inputs from the user.

Internal Input Widgets

11.2.4. Gauge Widgets

These are widgets commonly used for displaying values.

Internal Gauge Widgets



11.2.5. Label Widgets

These are widgets commonly used for displaying text information.

Internal Label Widget

11.2.6. Background Widgets

These are widgets commonly used for adding visual cues or design.

Internal Background Widgets

11.3. Inherent Widgets

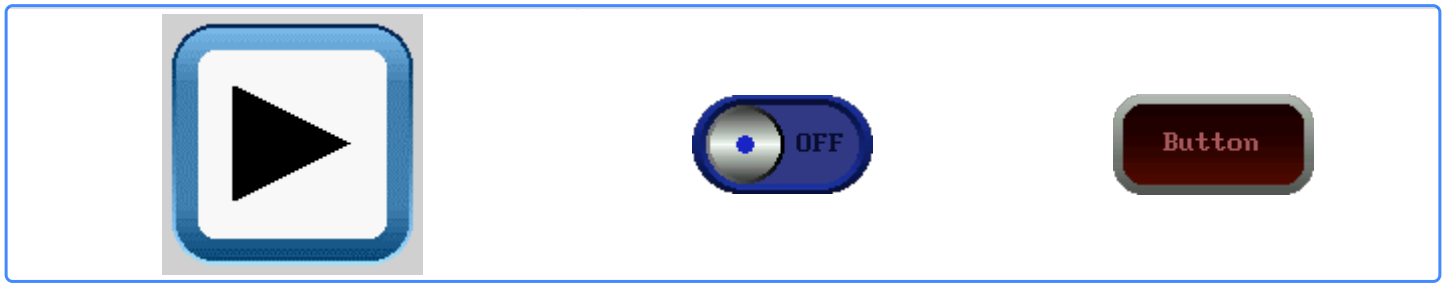
The Inherent widgets are widgets that are rendered in real-time by utilizing proprietary algorithm. These widgets are available in the standard version of Workshop4. For detailed discussion on this type of widgets, refer to the Workshop4 Widgets Reference Manual.

The following subsections show examples of these widgets.

11.3.1. Button Widgets

These are widgets commonly used for receiving touch inputs from the user.

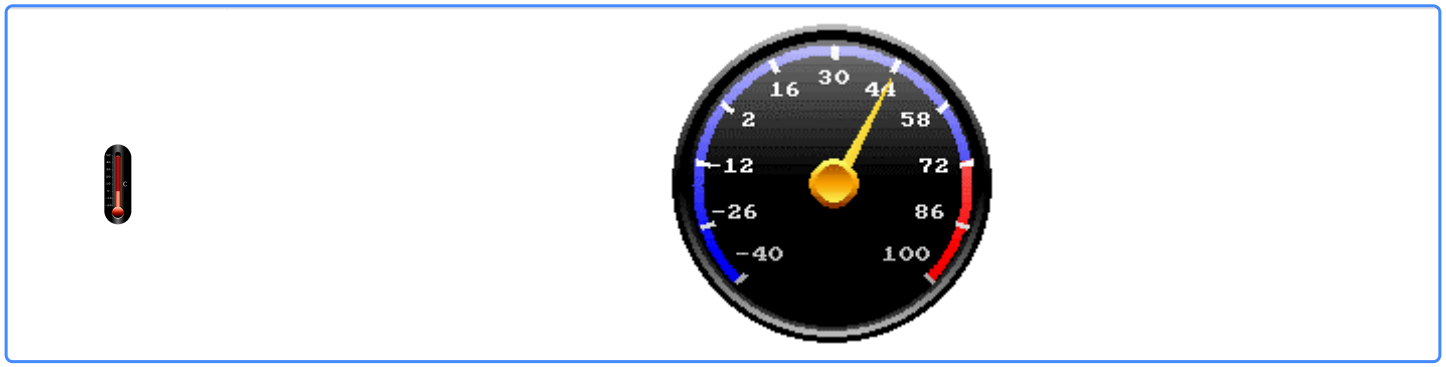
Inherent Button Widgets



11.3.2. Gauge Widgets

These are widgets commonly used for displaying values.

Inherent Gauge Widgets



11.3.3. Background Widgets

These are widgets commonly used for adding visual cues or design.

Inherent Background Widgets

11.3.4. Label Widgets

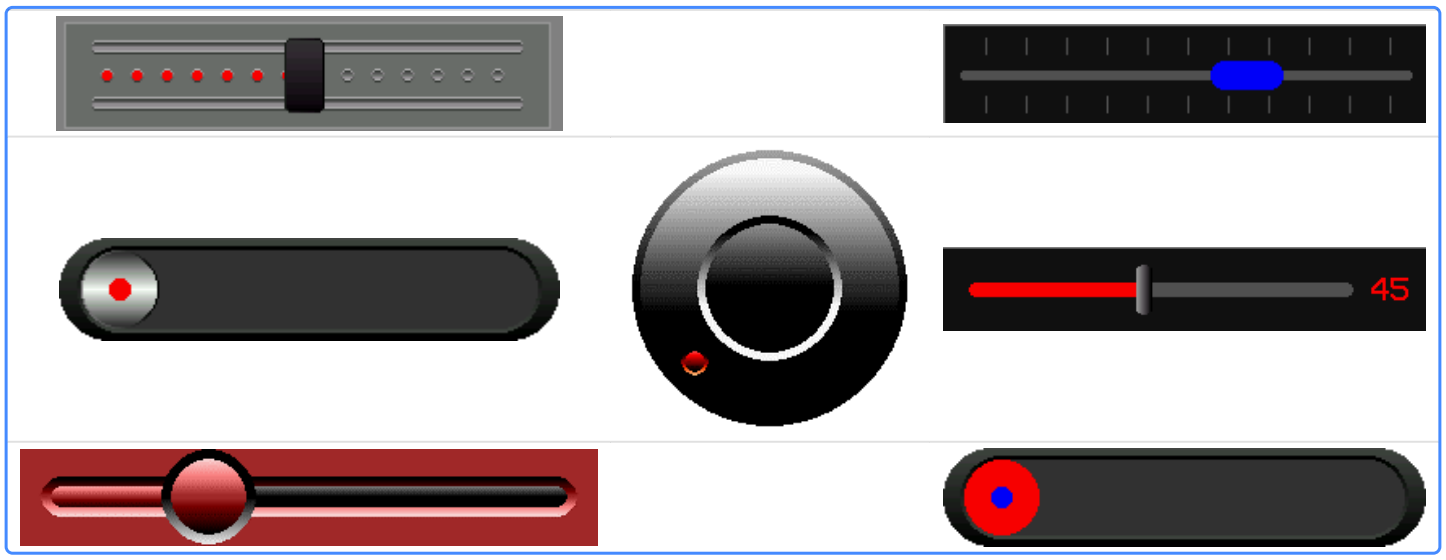
These are widgets commonly used for displaying text information.

Inherent Label Widget

11.3.5. Input Widgets

These are widgets commonly used for receiving touch inputs from the user.

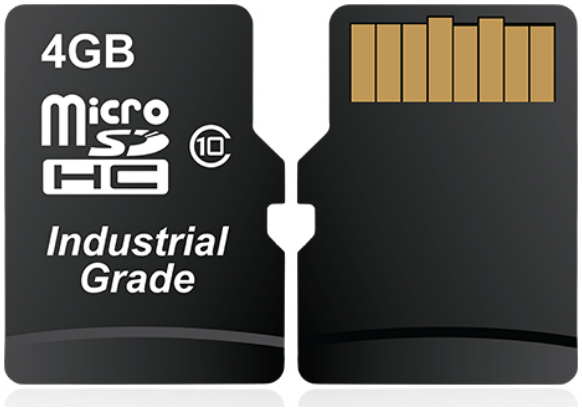
Inherent Input Widgets



12. Memory Cards

The PIXXI processor uses off the shelf standard SD/SDHC memory cards with up to 4GB capacity usable with FAT16 formatting. For any FAT file related operations, before the memory card can be used it must first be formatted with FAT16 option. The formatting of the card can be done on any PC system with a card reader. Select the appropriate drive and choose the FAT16 (or just FAT in some systems) option when formatting. The card is now ready to be used in the PIXXI based application.

The PIXXI processor also supports high capacity SDHC memory cards (4GB and above). The available capacity of SDHC cards varies according to the way the card is partitioned and the commands used to access it. Below is an image of a 4GB micro-SD memory card.



Industrial-Grade Micro-SD Card

The FAT partition is always first (if it exists) and can be up to the maximum size permitted by FAT16. Windows 7 or newer will format FAT16 up to 4GB. Windows XP will format FAT16 up to 2GB and the Windows XP command prompt will format FAT16 up to 4GB.

RMPET, a 4D Labs Tool found in the Workshop4, is capable of repartitioning and formatting microSD cards to be the appropriate type and format for 4D Labs processors. This should be used for all cards.

Note

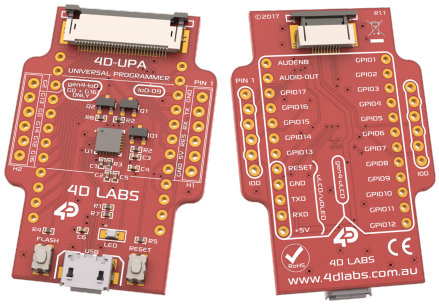
- A SPI Compatible SDHC/SD card MUST be used. PIXXI along with other 4D Labs Processors requires SPI mode to communicate with the SD card. If a non-SPI compatible SD card is used, then the processor will simply not be able to mount the card.
- Read disturb is a well-known issue with flash memory devices, such as micro-SD cards, where reading data from a flash cell can cause the nearby cells in the same memory block to change over time. This can be prevented by using industrial-grade micro-SD cards with read disturb protection. Industrial-grade micro-SD cards have a firmware that actively monitors the read operation and refreshes areas of memory which have high traffic and even move data around to prevent read disturb error from occurring. Furthermore, manufacturers may choose to implement read disturb protection on a certain part of the flash memory only, such that the beginning part of the memory might not be protected. The RMPET utility in Workshop4 is designed to create the first partition at an offset from the start of the micro-SD card to account for this situation. It is therefore recommended to always partition and format an industrial micro-SD card using the RMPET utility prior to using it with 4D Labs processors.

13. Hardware Tools

The following hardware tools are required for full control of the PIXXI processor.

13.1. Programming Tools

The 4D-UPA Programming Adaptor (image shown below) is an essential hardware tool to program, customise, and test the PIXXI Processor.



4D-UPA Programming Adaptor

The 4D-UPA Programming Adaptor is used to program a new Firmware/PmmC, Display Driver and for downloading compiled 4DGL code into the processor. It can even serve as an interface for communicating serial data to the PC.

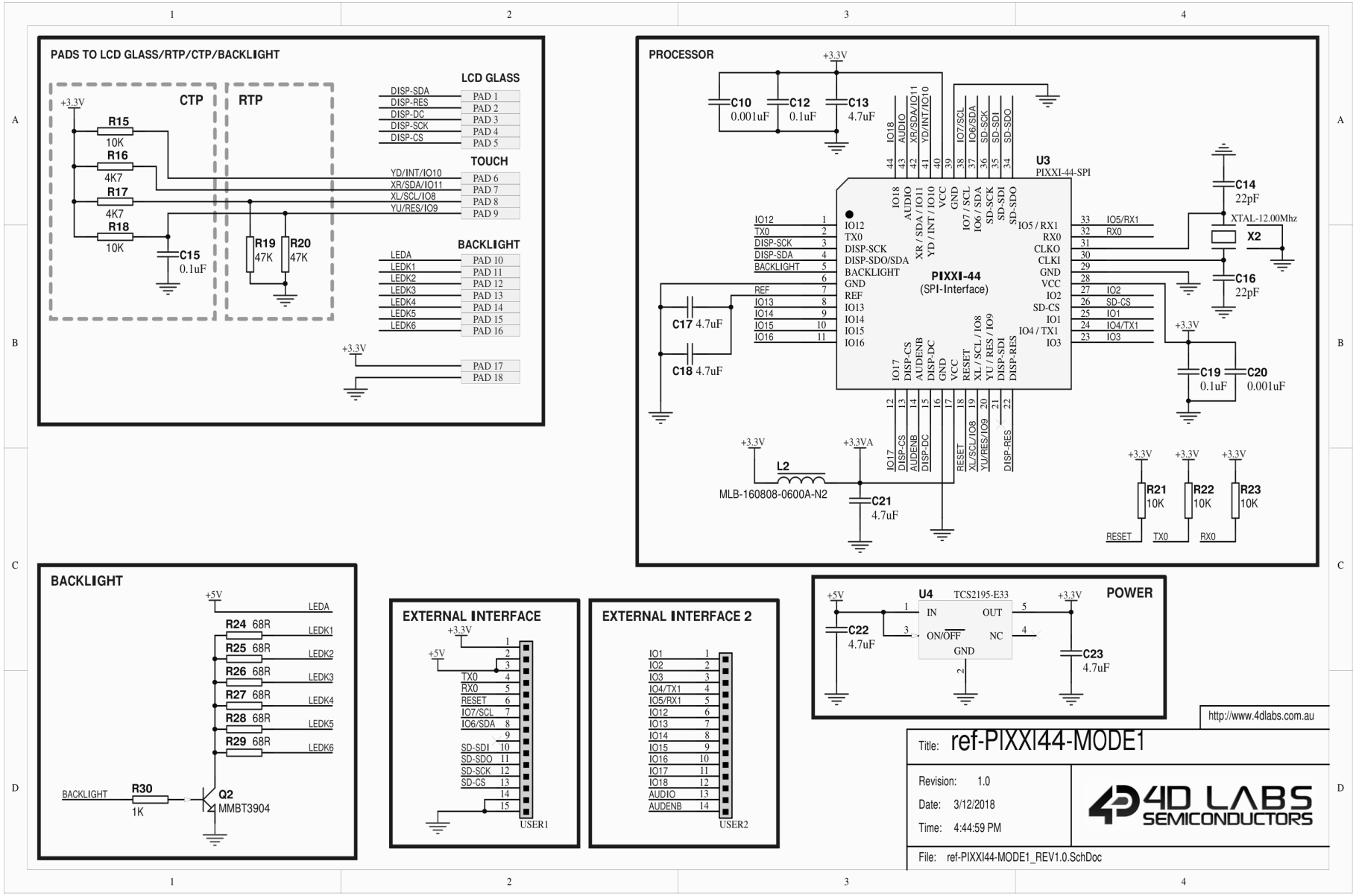
The 4D-UPA Programming Adaptor is available on the 4D Systems website.

> **Note**
>
> Using a non-4D programming interface could damage your processor and void your Warranty.

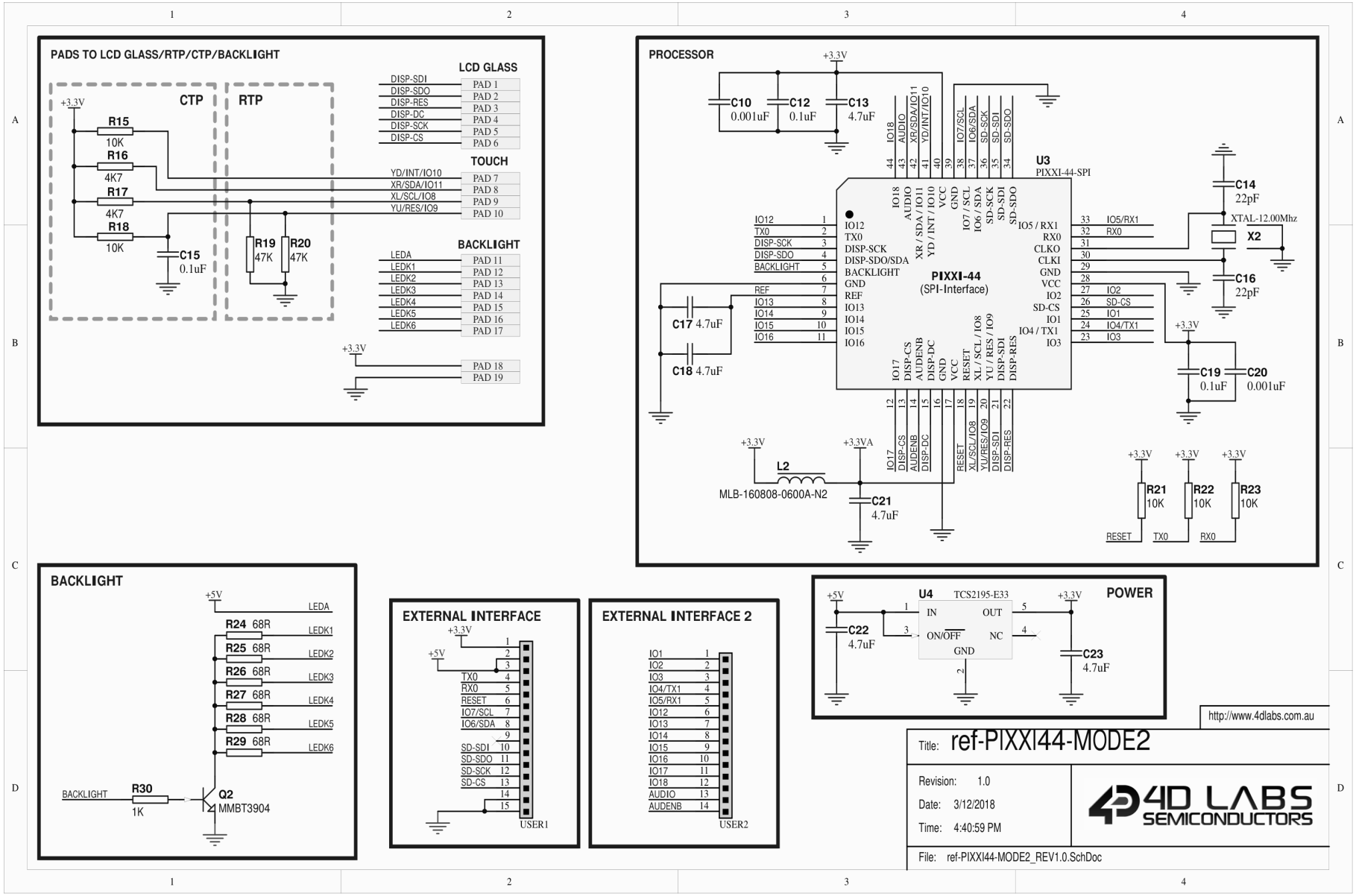
13.2. Starter Kits and Evaluation Modules

Various starter kits and modules are available from 4D Labs to evaluate the features of the PIXXI-44. Please check with your local supplier.

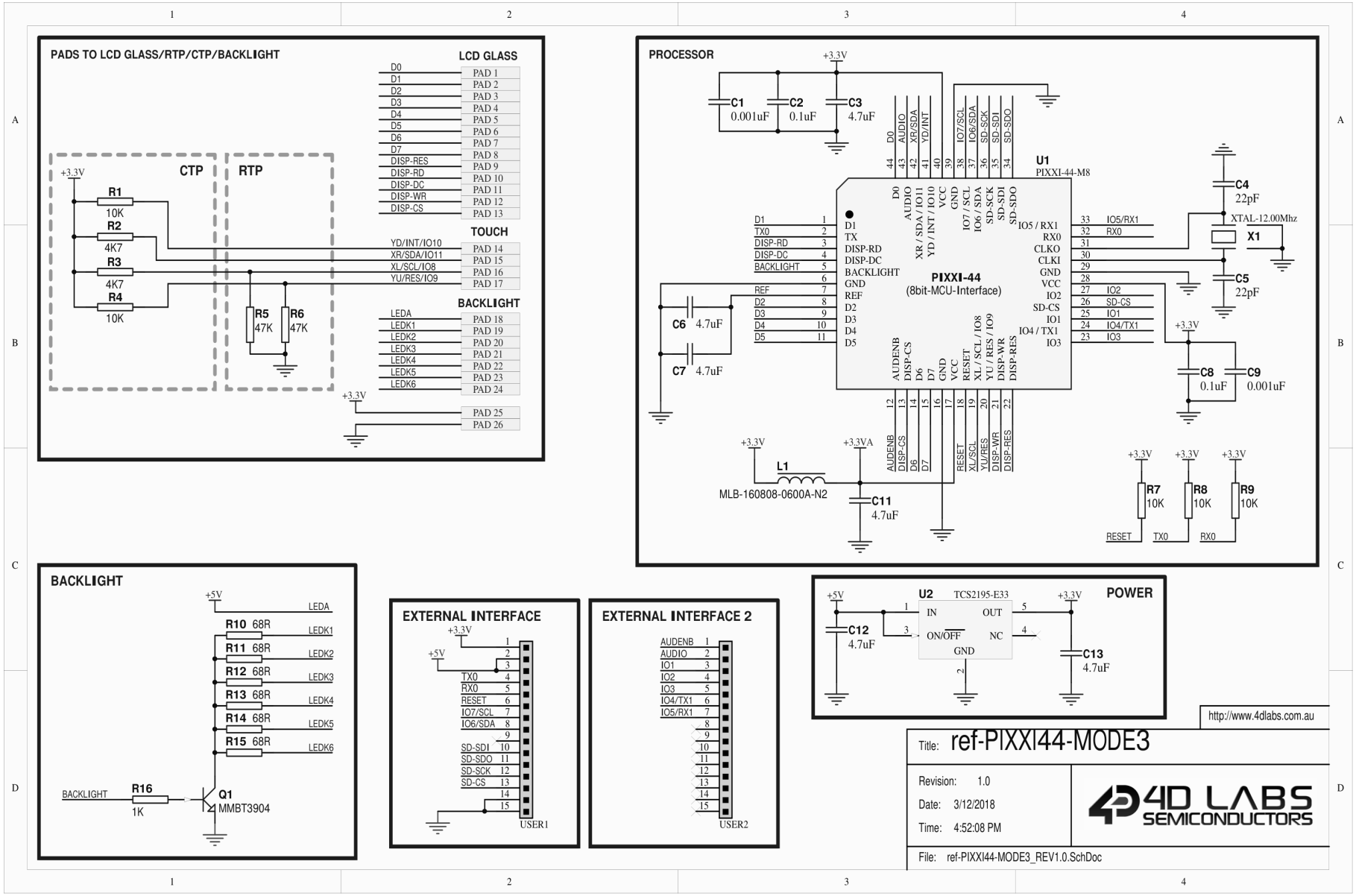
14. Reference Design for PIXXI-44 (Mode-1)



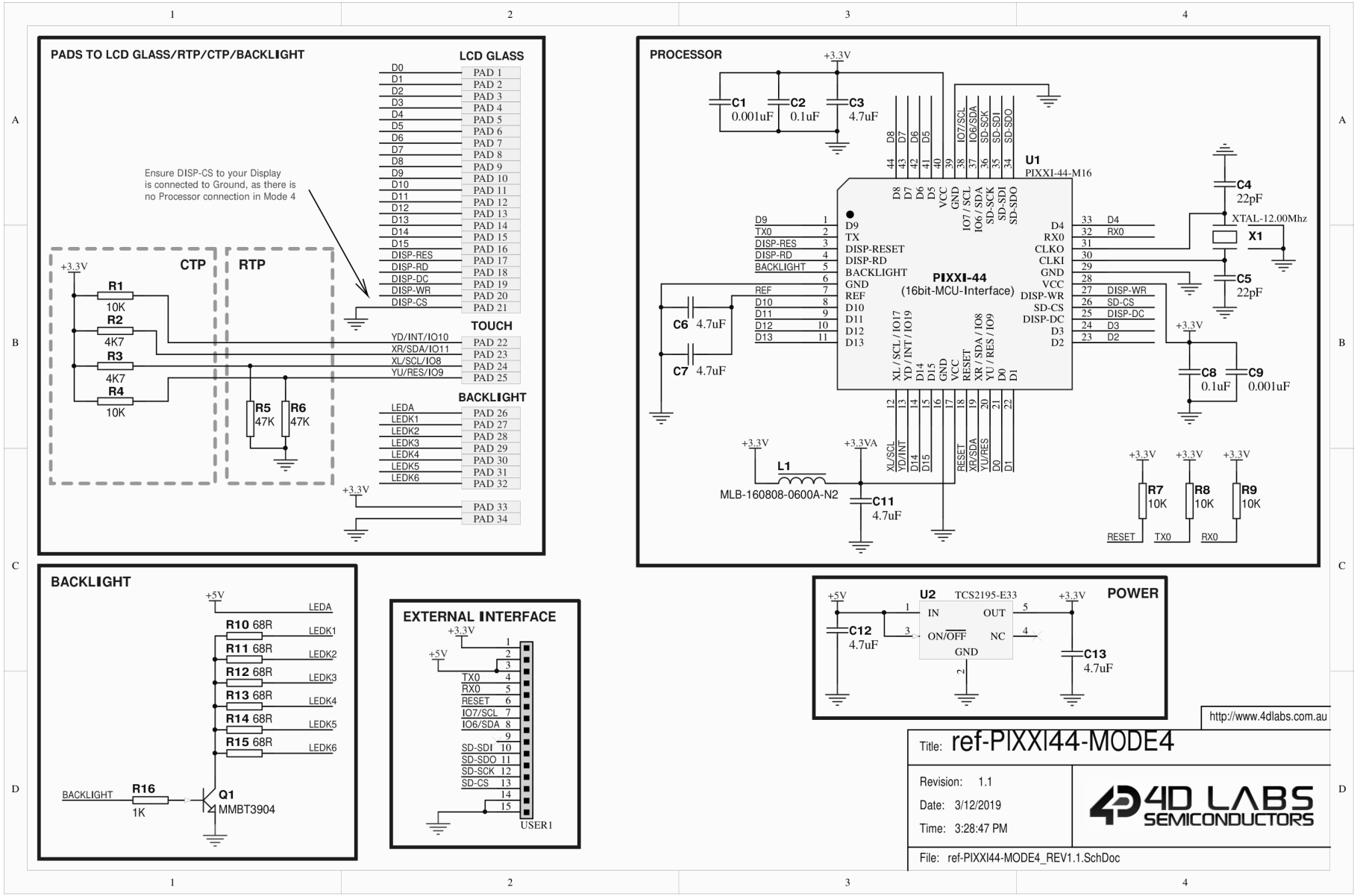
15. Reference Design for PIXXI-44 (Mode-2)



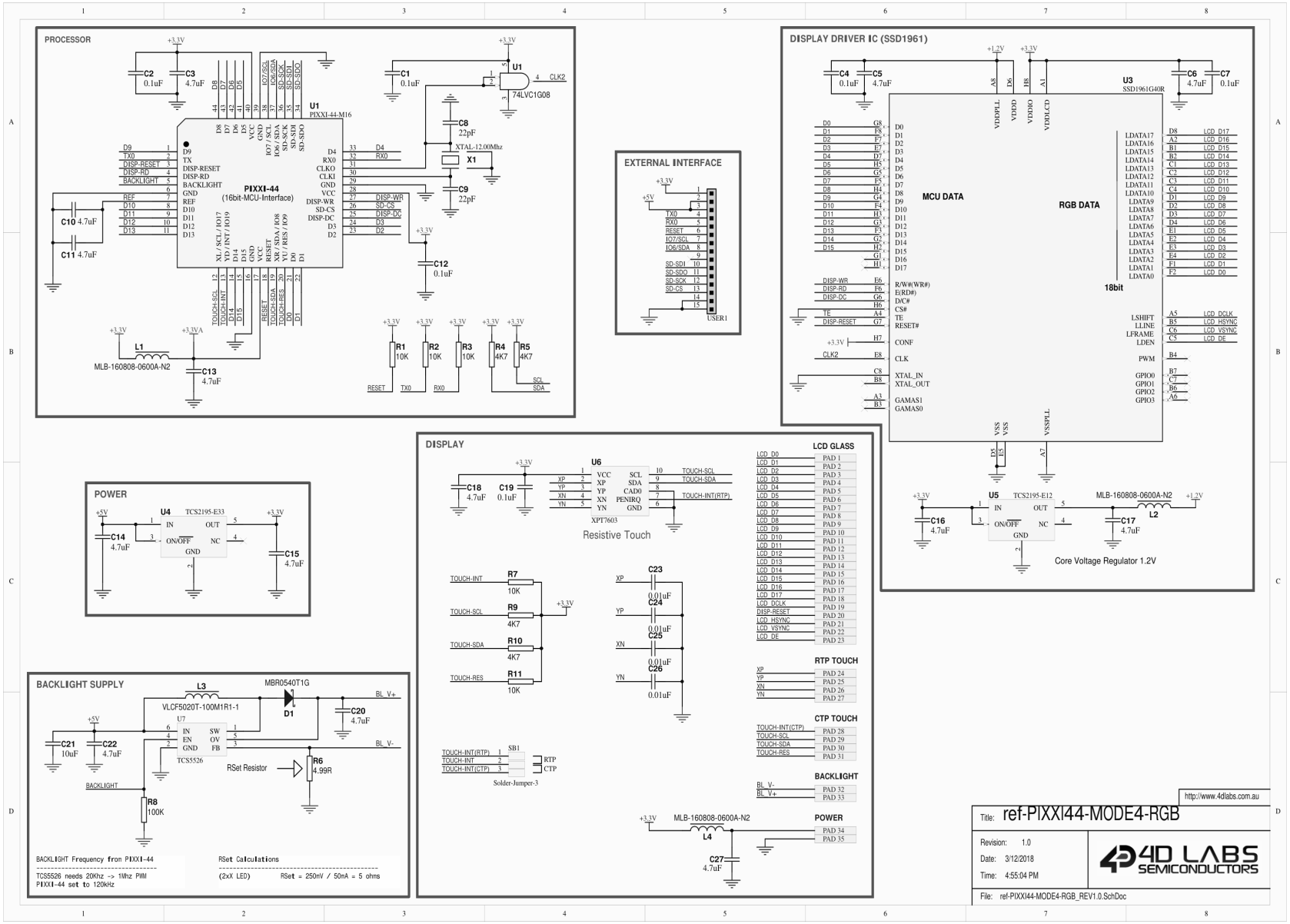
16. Reference Design for PIXXI-44 (Mode-3)



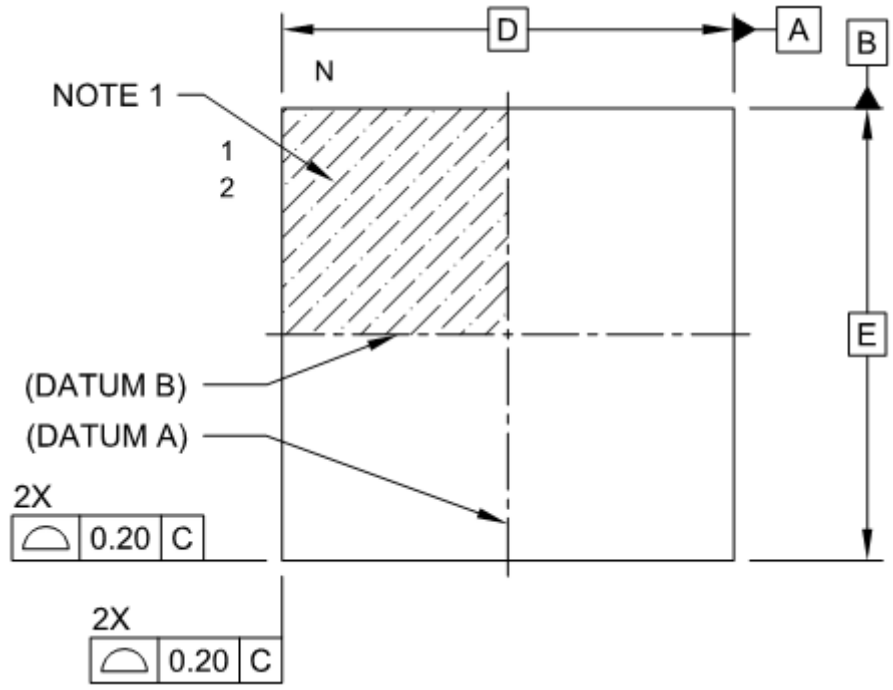
17. Reference Design for PIXXI-44 (Mode-4)



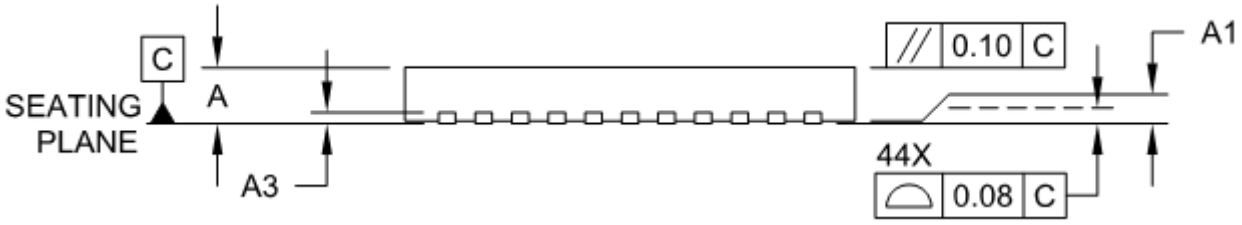
18. Reference Design for PIXXI-44 (Mode-4 RGB 16-bit using an RGB Video Driver IC)



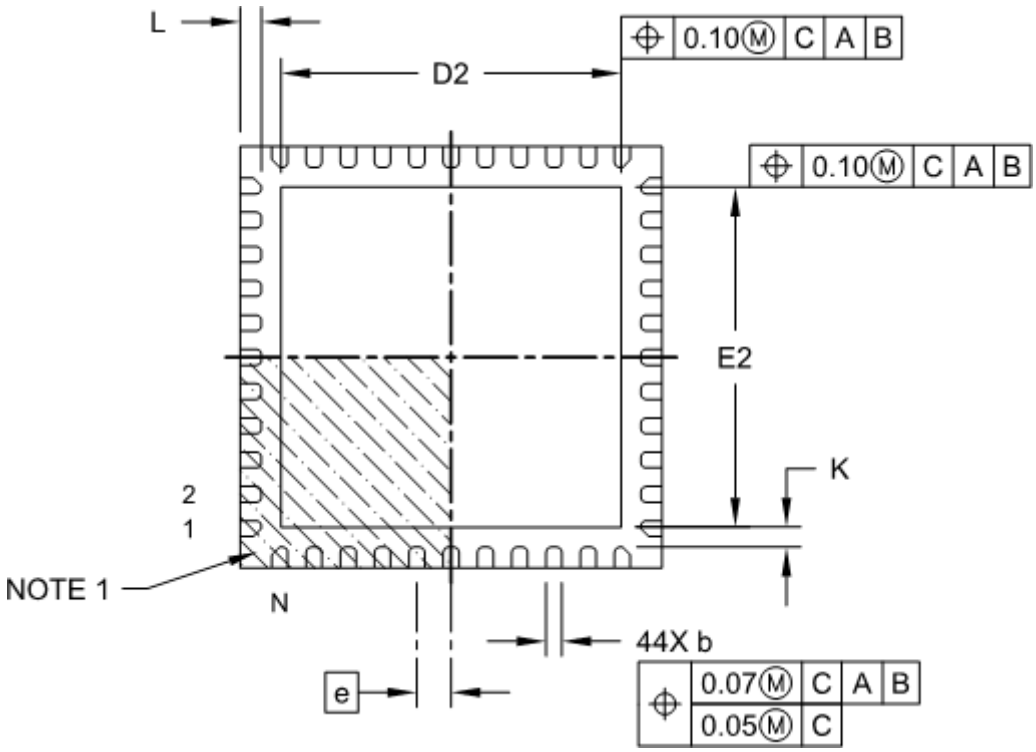
19. Package Details



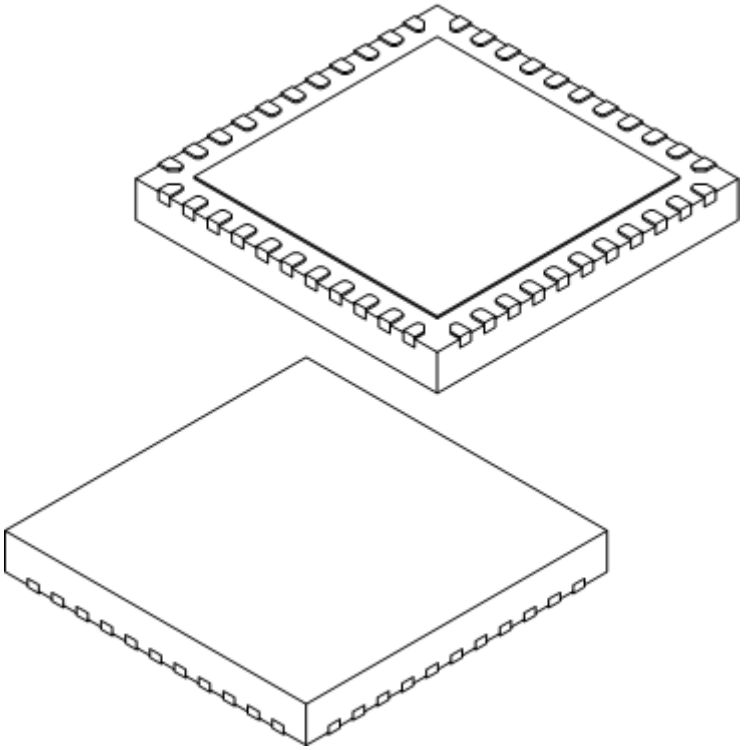
Top View



Side View



Bottom View



Isometric View

Package Dimension Details

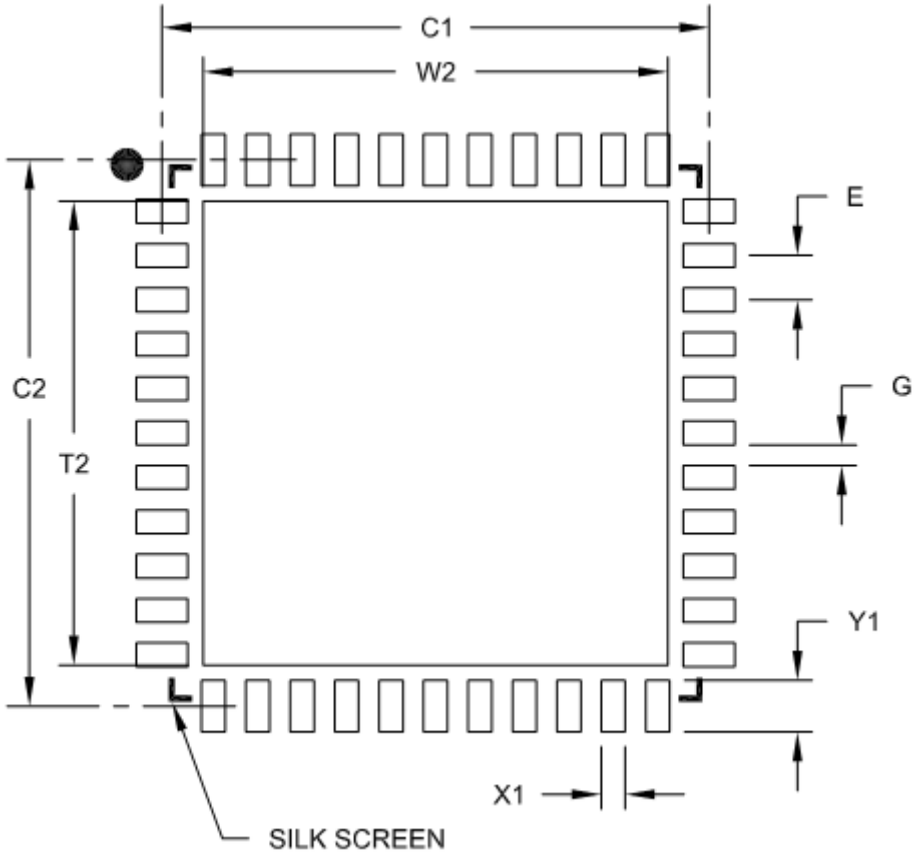
Dimension Limits		Min (mm)	Nom (mm)	Max (mm)
Number of Pins	N	44		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Width	E	8.00 BSC		
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D	8.00 BSC		
Exposed Pad Length	D2	6.25	6.45	6.60
Terminal Width	b	0.20	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed Pad	K	0.20	-	-

Note

1. Pin 1 visual index feature may vary but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
    - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    - REF: Reference Dimension, usually without tolerance, for information purposes only.

20. PCB Land Pattern

Shown below are the recommended land pattern and measurement details for the PIXXI-44 processor.



Recommended Land Pattern for PIXXI-44

Measurement Details for Land Pattern

Dimension Limits		Min (mm)	Nom (mm)	Max (mm)
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Center Pad Spacing	C1		8.00	
Center Pad Spacing	C2		8.00	
Contact Pad Width	X1			0.35
Contact Pad Length	Y1			0.85
Distance Between Pads	G	0.25		

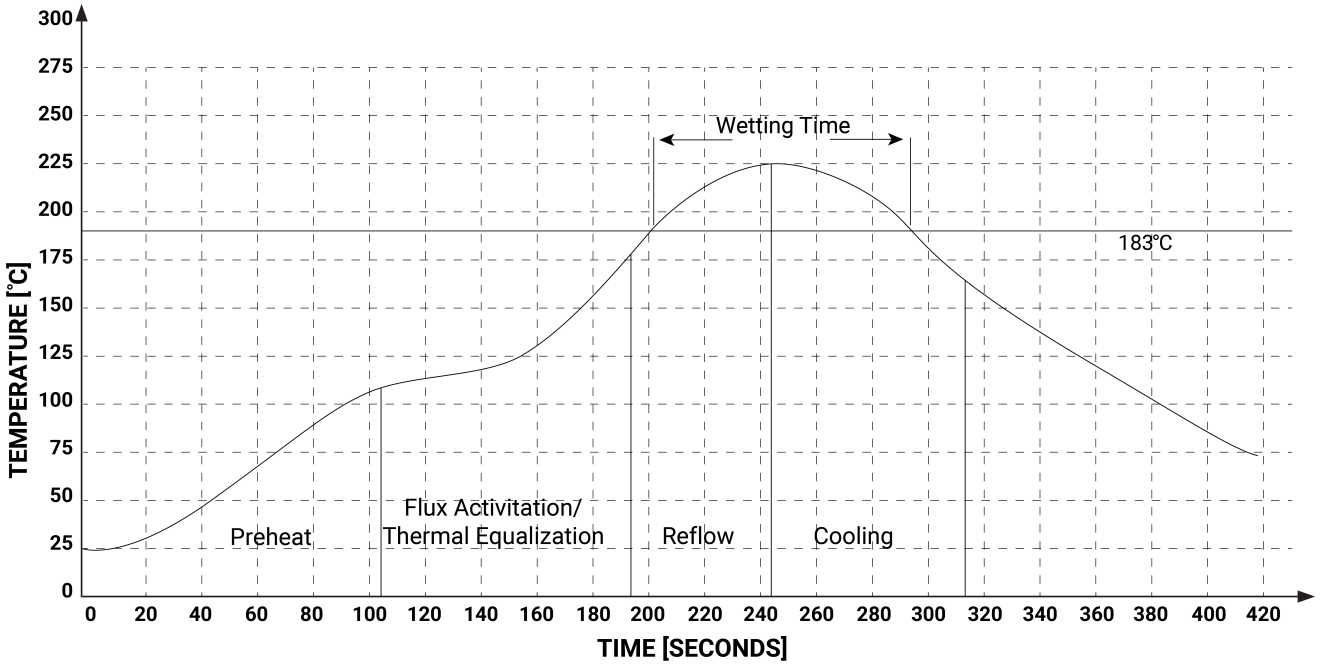
Note

1. Dimensioning and tolerancing per ASME Y14.5M.
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

21. Solder Reflow Recommendation

This section discusses the **Lead (Pb) free** solder reflow process and recommendations.

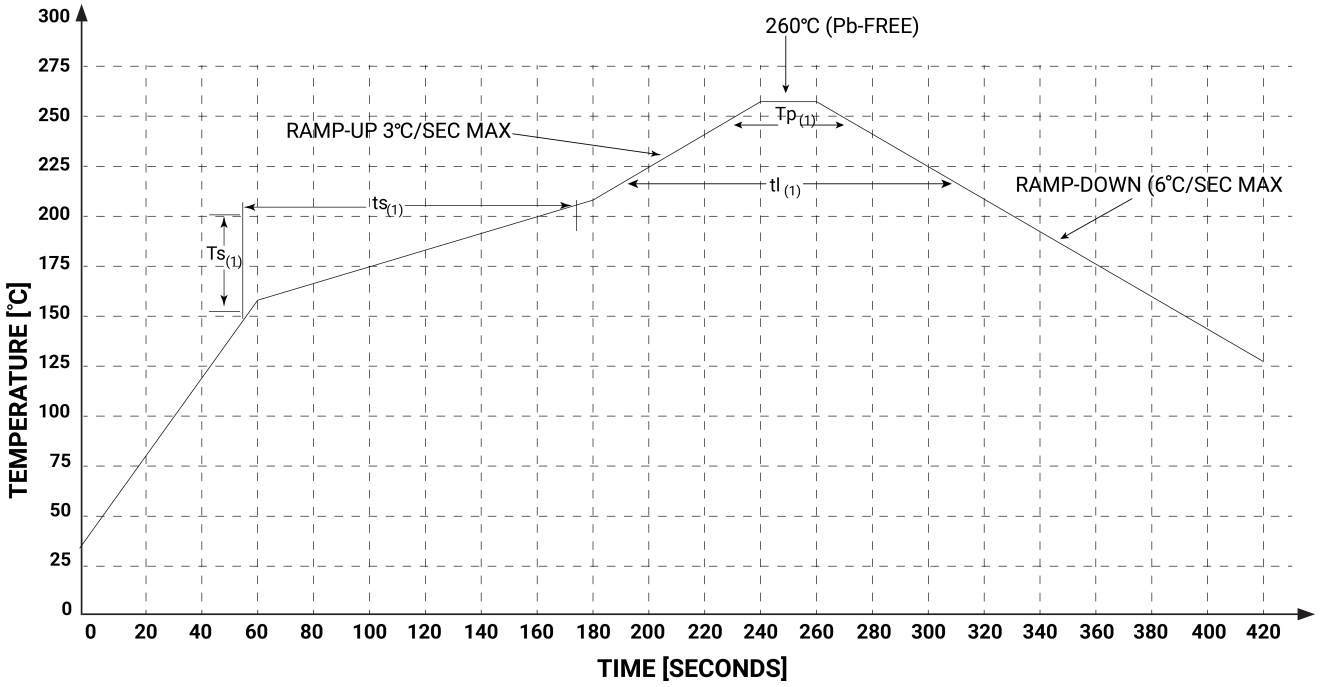
The solder reflow process typically undergoes five transition periods as shown in the diagram.



1. **Preheat** – Elevates the assembly's temperature from 25°C to 80-150°C, facilitating the evaporation of solvents from the solder paste.
2. **Flux Activation** – The dried solder paste undergoes heating to a temperature that activates the flux, enabling it to react with oxides and contaminants present on the surfaces intended for joining.
3. **Thermal Equalization** – Aims to achieve temperature uniformity, typically around 25-50°C below the reflow temperature. The specific time and temperature required depend on factors such as the mass and materials involved.
4. **Reflow** – In this phase, the assembly is heated to a temperature sufficient for solder reflow. Notably, the "wetting time" indicates the duration during which the solder remains in a liquid state, typically around 183°C on the curve.
5. **Cooling** – This marks the concluding stage of the process, emphasizing gradual cooling for optimal results. A slower cooling rate promotes the formation of a finer grain structure in the solder joint, enhancing its resistance to fatigue.

21.1. Jedec Reflow Profile

Reflow conditions from IPC/JEDEC J-STD-020C are reproduced in the following diagram and table.

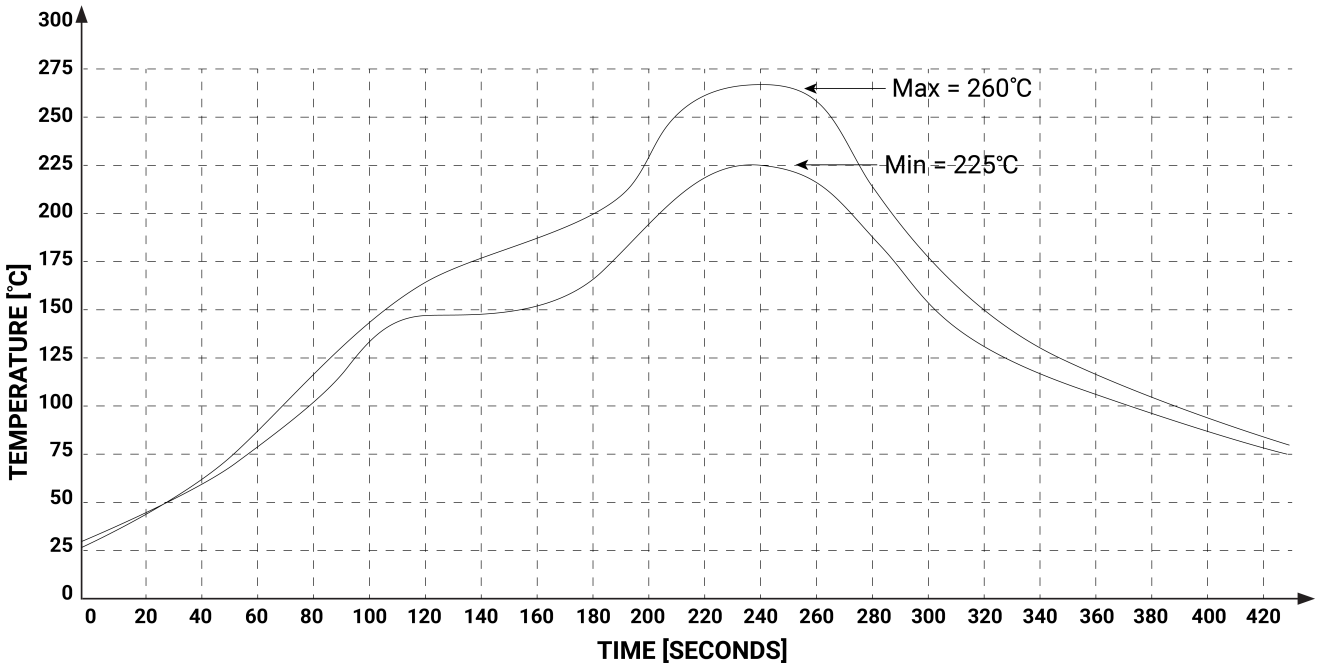


Time and Temperature Parameters

Symbol	Min	Max	Units
Ts	150	200	°C
ts	60	180	seconds
tl	60	150	seconds
Tp	225	240	°C

21.2. Reflow Profile Recommendation

The illustration below illustrates the suggested profiles for Pb-free devices. These devices are coated with matte Tin (Pure Sn) and are free of lead content. They are suitable for use in standard tin-lead (SnPb) applications, provided the profile meets or exceeds the lower line in the plot. Alternatively, they can be utilized in Pb-free solder, such as Tin-Silver-Copper (Sn-Ag-Cu), with profiles falling within or below the upper line on the plot.



22. Specifications and Ratings

The tables below show the absolute maximum ratings, recommended operating conditions, and global characteristics based on operating conditions of the processor.

Absolute Maximum Ratings

Operating ambient temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on VCC with respect to GND	-0.3V to 4.0V
Maximum current out of GND pin	300mA
Maximum current into VCC pin	300mA
Maximum current sunk/sourced by any pin	15mA
Total power dissipation	1.0W

Note

Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the recommended operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage (VCC)		3.0	3.3	3.6	V
Operating Temperature		-40	-	+80	°C
External Crystal (Xtal)		-	12.00	-	MHz
Input Low Voltage (VIL)	VCC = 3.3V, all pins	VGND	-	0.2VCC	V
Input High Voltage (VIH)	VCC = 3.3V, non 5V tolerant pins	0.8VCC	-	VCC	V
Input High Voltage (VIH)	5V-tolerant pins, RX0 and TX0 pins only	0.8VCC	-	5.5	V

Global Characteristics Based on Operating Conditions

Parameter	Conditions	Min	Typ	Max	Units
Supply Current (ICC)	VCC = 3.3V	-	40	60	mA
Internal Operating Frequency	Xtal = 12.00MHz	-	70.00	-	MHz
Output Low Voltage (VOL)	VCC = 3.3V, IOL = 3.4mA	-	-	0.4	V
Output High Voltage (VOH)	VCC = 3.3V, IOL = -2.0mA	2.4	-	-	V
A/D Converter Resolution	XR, YU pins	8	-	10	bits
Capacitive Loading	CLK1, CLK2 pins	-	-	15	pF
Capacitive Loading	All other pins	-	-	50	pF
Flash Memory Endurance	PmmC Programming	-	10000	-	E/W

23. Revision History

Datasheet Revision

Revision Number	Date	Description
1.0	24/01/2020	Initial release version
1.1	30/06/2020	Widget term updates, and Widget document name change
1.2	16/07/2020	Updated Device Configuration Mode Status for current availability
1.3	24/08/2022	Updated Mode-1 and Mode-2 pinout for TX1 - Fixed error in voltage tolerance on IO6/IO7/Flash-SDI to be 3.3V. - Updated Mode-1 and Mode-2 Pinout images. - Enabled Mode-2 as that is now a released Mode.
1.4	31/10/2023	Modified datasheet for web-based documentation.
1.5	12/03/2024	Updated formatting for resource centre redesign
1.6	08/05/2024	Added solder reflow recommendation section

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